DETERMINATION OF SEMICONDUCTOR DEVICE CHARACTERISTICS USING MICROPROCESSOR

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MASTER OF TECHNOLOGY

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A. S.

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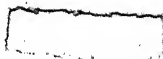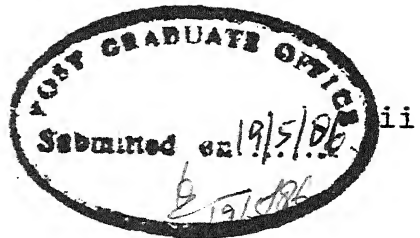
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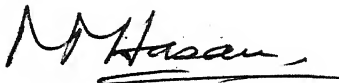
MAY, 1986

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CERTIFICATE

CERTIFIED that the thesis entitled 'DETERMINATION OF SEMICONDUCTOR DEVICE CHARACTERISTICS USING MICROPROCESSOR' has been submitted by A.S. Chitale under my supervision and that this work has not been submitted elsewhere for award of a degree.

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ABSTRACT

The title of the thesis is ' Determination of Semiconductor Device Characteristics Using Microprocessor'. The measurement system has been designed using 8085A-based Microprocessor Workstation locally developed. The system is capable of obtaining characteristics of a wide variety of semiconductor devices like BJTs (Bipolar Junction Transistors) and FETs (Field Effect Transistors). The design philosophy has taken into consideration the differences in the operating principles of different types of devices. Care also has been taken to avoid the effect of measurements themselves on the desired characteristics.

Different characteristics such as I_C-V_{CE}, β-I_C, V_{BE}-I_B for BJTs and I_D-V_{DS}, g_m-V_{DS}, I_D-V_{GS} etc. for FETs have been implemented. Facility for hardcopy output in the form of X-Y plots has also been designed. Test results using the system have been obtained and compared with the actual characteristics. Further improvements have also been suggested. The system gives modest accuracy in the measured data . Suggestions have been made for the improvement of the measurement system.

CHAPTER I

INTRODUCTION

Ever since the introduction of microprocessors, a wide variety of problems have been addressed to them to make things easier and more convenient for everybody- a layman as well as a scientist. Sophisticated electronic systems using a considerable amount of random logic hardwired to form a specific system have been replaced by microprocessor based systems applying program control operation. The feasibility of modifying the control programs also increases the system flexibility and functional capability. In addition, such systems have advantages such as reduced costs, higher reliability, etc. These systems not only allow a comprehensive testing procedure to be applied, but also provide flexibility and versatility for future system modifications with minimal physical modifications [1].

This work proposes to apply the vast capabilities of Microprocessor based systems to determine static characteristic of semiconductor devices.

One main problem that a technical user of any engineering component-electronic, electrical or mechanical- may face is the lack of actual characteristics of the component. This is particularly true for a user of electronic devices such as transistors for more than one reasons.

These reasons fall into the following categories [2].

(a)   The measurements are for providing better components.
During the development of a circuit, the designer needs to
know the actual characteristics of transistors being used
for the best results.Similarly during the design phase of
each device, after each design iteration, the designer
requires the determination of parameters in a rapid and pre-
cise manner.   These are the main motivations for development
of an automatic characteristic acquisition system controlled
by a microprocessor.

(b)   The information given by a data sheet is typical. Thus
for different pieces of the same type of component, the para-
meter values may vary over a wide range.   Thus such measurement
also help in sorting of components.

(c)   They can also be used for predicting the performance of
a circuit as also for improving it.   Moreover, such measurement
also provide a good analytical information for engineers impro
ving component design and specifications.
The reasons make it very much necessary to obtain device
characteristics accurately and quickly.

        In this thesis work the main aim has been to
obtain the actual characteristics of most commonly used
three terminal devices such as BJTs (NPN,PNP) and FETs (n-
channel,p-channel).

Most of the important static characteristics such as I_C - V_{CE}. β - I_C, I_B - V_{BE} etc for BJTs and I_D - V_{DS}, I_D - V_{GS}, g_m - I_D etc. for FETs can be obtained easily and quickly. The hardcopy of the characteristics can be obtained by attaching X-Y plotter to the system. The hardware and software have been developed to make the whole system automatic with minimum manual interaction . The convenience of the user has been the main consideration.

Chapter II gives a broad idea of the hardware employed and its interface with the Microprocessor Workstation and the X-Y plotter . While designing the hardware and control section, the differences between BJT and FET have been carefully considered and taken care of, the main one being that while BJT is a current controlled device, FET (Field Effect Transistor) is a voltage controlled device, as the name suggests. It also describes the circuit employed for switching between the control sections of FET and BJT and the Data Acquisition Circuitry.

Chapter III describes the software stored in EPROM (Ultra Violet Erasable Programmable ROM). It also describes software techniques for discontinuous driving of devices. This is required since a continuous application of voltages and currents may lead to excessive heat generation which may alter significantly the characteristics of the semiconductor device under measurement. Interrupting the

applied currents and voltages frequently thus helps keep the internal temperature down [2].

Chapter IV describes the software and hardware interfacing and shows how the software controls the hardware for desired operation.

Chapter V discusses the test results of the system and the accuracy of the system. It will also cover the limitations of the system and suggest further inclusions and deletions and improvement to be incorporated in the system.

CHAPTER II

HARDWARE DESCRIPTION AND IMPLEMENTATION

2.1 INTRODUCTION:

In any microprocessor based measurement
system, the user is only involved with the software inter-
face provided to him. However, the real data retrieval
and measurement work is carried out by the target hardware
which is being driven by the software stored in EPROM.
Hence the hardware of the system does the main job of
applying test signals and retrieving the information of
interest, albeit under software control. Hence the choice
of hardware becomes very important.

The final specifications of the system will depend
on the specification of hardware used. Specification like
accuracy, resolution, sensitivity will depend to a great
extent on the hardware components used. The limitations
of the hardware are essentially the limitations of the
system. So it is of great interest to look into the hard-
ware and its working.

An attempt has been made here to describe the
hardware employed. The chapter has been divided into three
sections.

(1)   Schematic Representation of the system.

(2)   The actual hardware employed for the realization of
       each of the functional modules and its justification.

(3)   The alternate method for carrying out the measurements:
       its advantages and disadvantages.

2.2   SCHEMATIC REPRESENTATION OF THE SYSTEM:

       The description of any measurement system should
identify the fundamental measurement functions, explain them
and link them with specific parts of the system. The operation
of any complicated measuring system can then be most unders-
tandably presented by dividing it into its basic functional
components or elements and grouping them into logical classi-
fications.

       This leads to a schematic diagram of the system
under study. It can be broadly presented as in Fig. 2.2.1.

       The measurement system developed has been based
on Microprocessor Workstation developed at I.I.T., Kanpur.
Each workstation consists of an 8085A based microprocessor
system, various interfaces for digital and analog input/
output and a video terminal for user interaction (see
Appendix I).

       The memory shown (Fig. 2.2.1) is the workstation
memory. A part of the memory is available for storage of
data retrieved during measurement.

       The interface of the measurement system with
the workstation is through a 44- pin edge connector which
carries the processor bus comprising of address, data and
control buses.
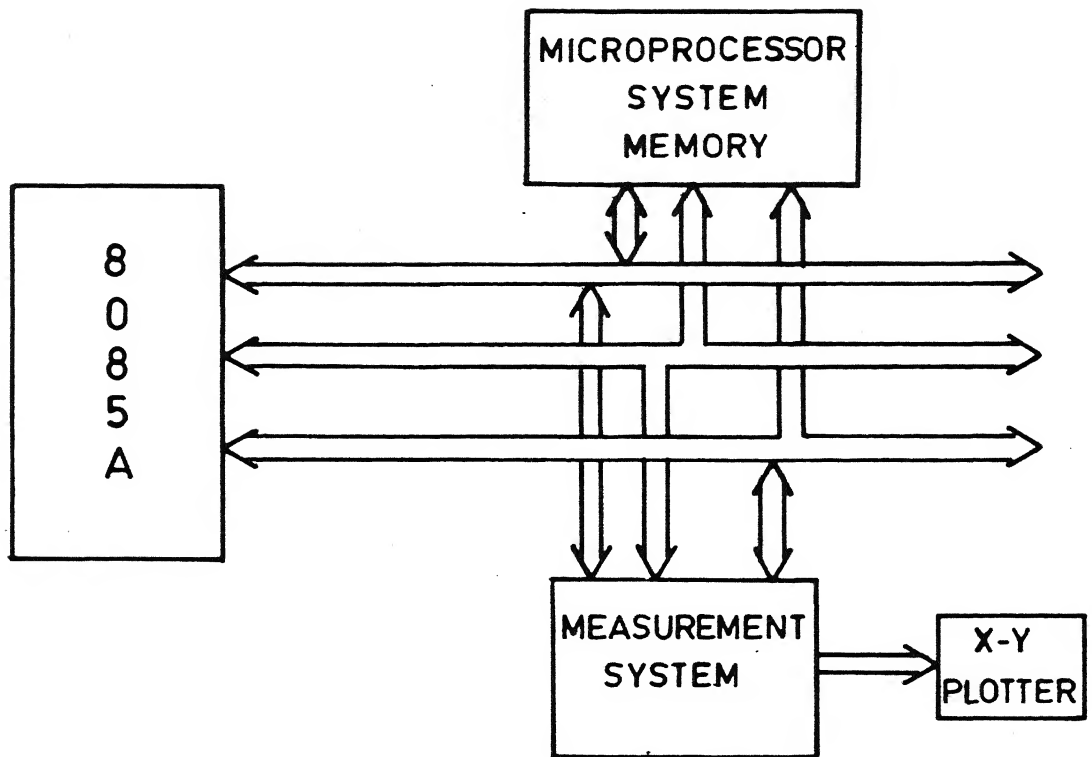
Fig. 2 : 2.1 Representation of measurement system.
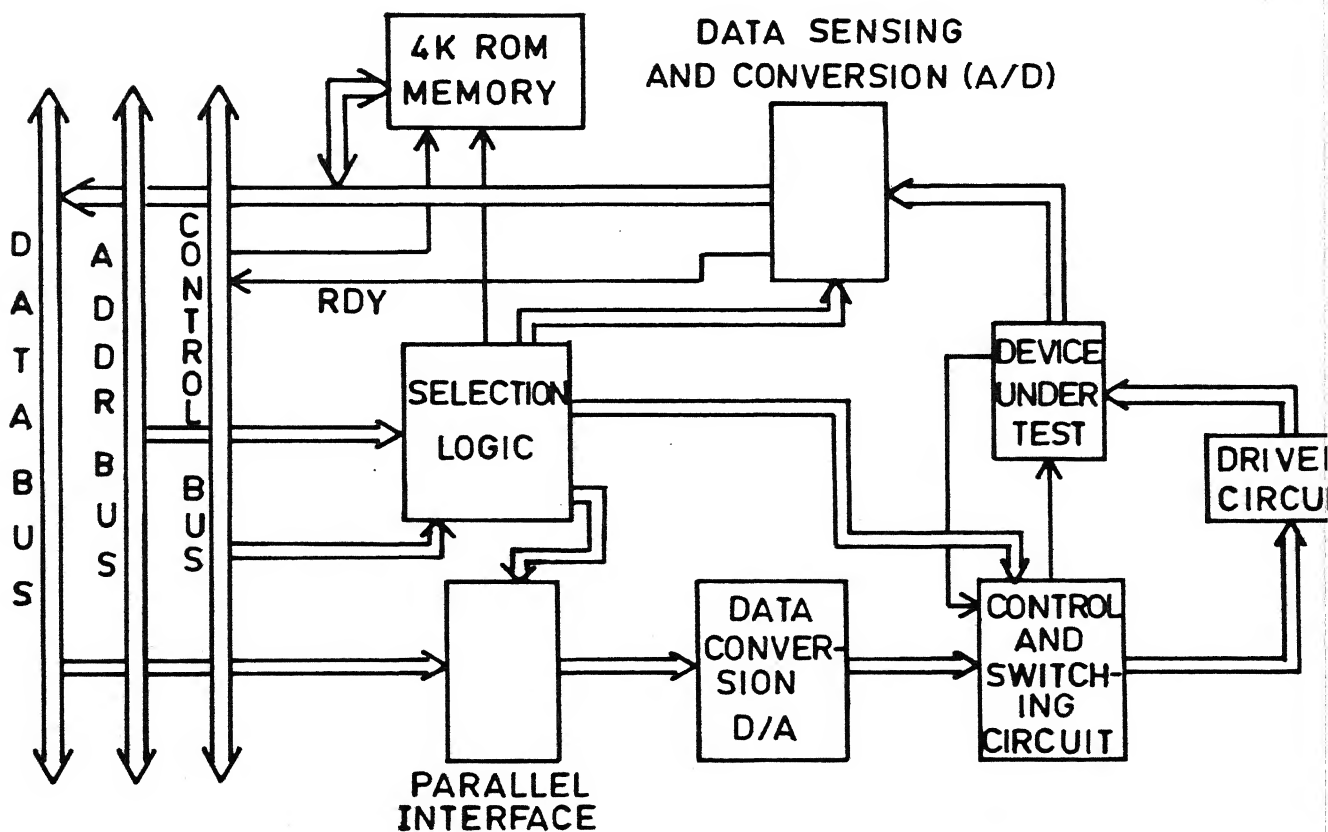
The X-Y plotter, which is required to provide an on-the-spot hardcopy of the characteristics measured, can be connected to the measurement system directly through a 5 pin connector. The X-Y plotter used is a Hewlett-Packard HP 7015B plotter.

The measurement system under study (hereafter referred to as ' the system' unless specified differently) can itself be subdivided into further logical blocks (Fig. 2.2.2). The block diagram clearly shows the method in which the system hardware is implemented.

The desired device characteristics can be defined as given below.

For a three terminal device, there are at the most three voltage and three current parameters. The device characteristics are obtained by making two parameters independent and one dependent, keeping all other parameters constant.

For one fixed value of one of the independent parameters, hereafter called the control parameter, the other independent parameter can be varied over a range of values and the effect on the dependent parameter observed.

Different sets of such measurements obtained over different values of the control parameter give the set of desired characteristics.

Parallel Interface is the main interface module between the workstation and the measurement system.

This module logically consists of two channels with digital to analog data conversion. This analog data, which is present in the form of voltages, is then applied as two independent parameters (Fig. 2.2.2).

Depending on the type of device under test, however, the control and independent parameters are appropriately currents or voltages. Moreover, the polarities of these signals also have to be proper. This is taken care of by the Control and Switching module with the help of the Selection Logic.

For example, for common emitter mode $I_C - V_{CE}$ measurements of an NPN BJT transistor, the control parameter is current I_B which sinks into the base of the device. Moreover, the collector-emitter voltage V_{CE} is positive. For a PNP BJT transitor, V_{CE} is negative and I_B is sourced out.

Thus the control section is perhaps the most important hardware module.

The dependent parameter to be measured, which is dependent on the two independent parameters, is mostly current. This current is passed through a precision resistor. The voltage then developed across it (or the voltage which may be the dependent parameter, as in $V_{BE}-I_B$ for BJT) is then sensed by the A/D Data Conversion module which converts the analog information to digital form to be passed on to the microprocessor. This information is then processed

and interpreted by software.

The on-board memory is the 4 k byte ROM (EPROM) which stores the software routines developed for the system. The software drives the target system hardware and also provides a friendly user interface.

The Selection Logic does the address and control lines decoding and sends appropriate signals to different modules of the system. It operates the control and switching logic module so that the module sends out proper signals to the device under test. It signals the Parallel Interface module to read data from the workstation. It signals the A/D Data Conversion module to start conversion cycle. In short, it is important from time keeping point of view and for proper operation of different modules.

2.3 THE ACTUAL HARDWARE IMPLEMENTATION OF EACH MODULE:

This section considers the hardware implementation and design considerations of each module.

2.3.1 Parallel Interface Circuitry:

This circuitry provides the data interface between the workstation and the measurement system.

As mentioned earlier, there are two logical channels for the control and independent parameters whose outputs are in the form of voltages prior to appropriate voltage or current conversion.

In the system, in order to have a better
control over the variations of one of the independent
parameters, a third physical data channel is present
through which fine control is implemented (described later).

These three physical channels are three 8-bit
8282 data latches used to latch the data sent by the work-
station to these channels. These latches are treated as
3 output ports by the workstation (Table 4.1). Selection
logic generates Data Latch signals accordingly. The hardware
implementation is shown in Fig. 2.3.1.

Most systems requiring such programming of
two or three channels use special purpose parallel inter-
facing chips such as Intel 8255. However, for three output
channels and one input channel interface, as in the system,
8255 does not provide ideal interfacing as all the output
data have anyway to be latched because the data read on the
input channel depends on the data present on the output
channels of 8255. Hence in this system, three physically
different channels have been designed, each acting as a fully
independent output port.

2.3.2. The Digital to Analog Conversion Module:

This module converts the digital signals from
the input data latches to analog signals to be passed on
to the control and switching circuitry. It consists of three
Digital to Analog Converters (DACs), one for each channel
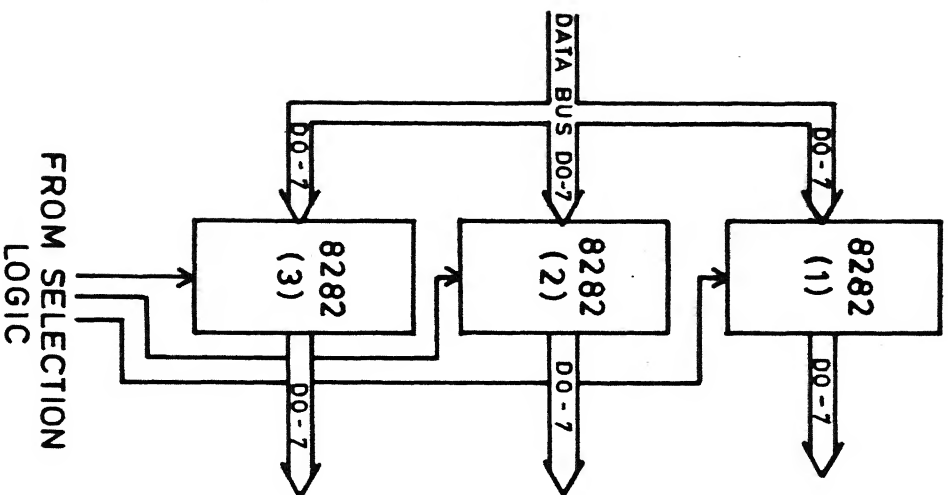
Fig.2:3.1 Parallel interface
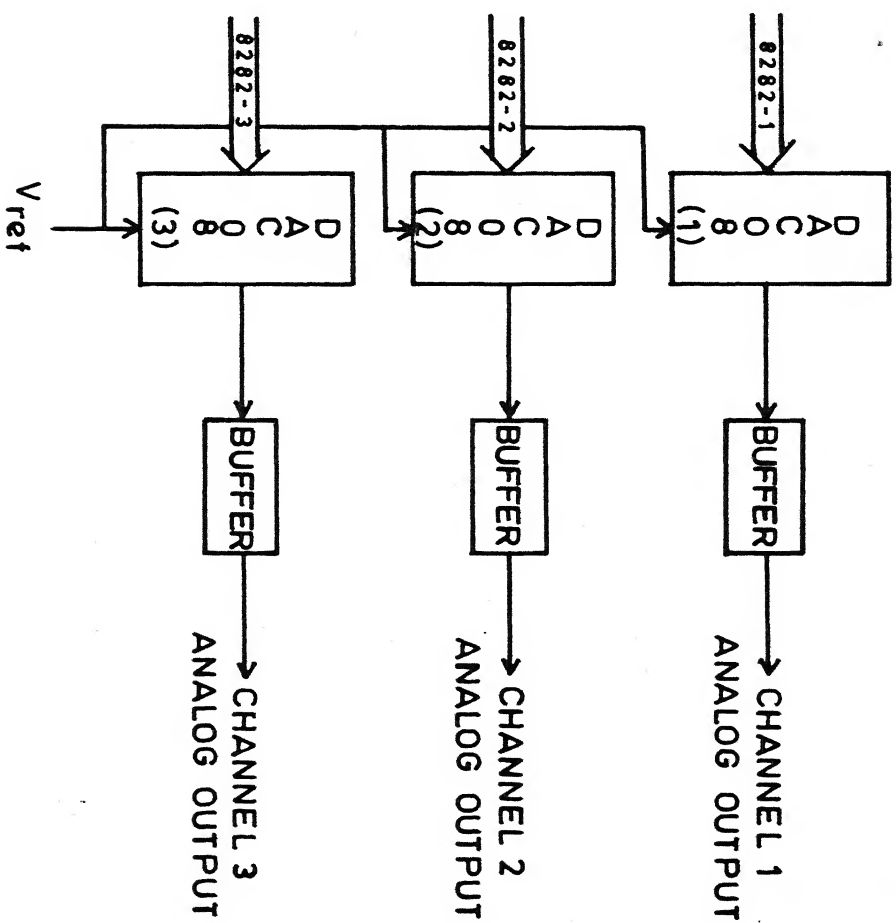
Fig.2:3.2 Digital to analog conversion.

(Fig. 2.3.2). The DACs used are ADDAC -08.

The DAC is a very important component of the system because it can affect the overall resolution and accuracy of the measurement system. So a little discussion of DACs will be in place.

Resolution of any DAC is defined as the number of output voltage steps it is capable of giving [3]. For ADDAC-08, which accepts 8 input bits, the number of possible output levels is $2^8 = 256$. Hence the smallest possible change in the output voltage, and consequently in any parameter due to DAC alone, is $1/2^8 = 0.4\%$ of full scale output. (However, scaling down of the output can be done with the help of operational amplifires and hence better resolution can be obtained, as has been implemented for fine control of one of the parameters).

To study the accuracy of a DAC, the DAC output voltage equation has to be analyzed. The equation of N-bit DAC output voltage is given below [3].

$$V_o = (2^{N-1}a_{N-1} + \cdots + 2^1.a_1 + 2^0.a_o) \times \frac{V_R}{2^N}$$

where,

V_R = stable reference voltage provided to DAC.

a_k = kth bit a_k = 0 if bit '0'

a_o = L.S.B.   = 1 if bit '1'

Thus the accuracy of the DAC depends on the accuracy and stability of the reference voltage provided to it an

the linearity of the DAC.

The reference voltage in the system is provided
by a buffered 10V zener diode reference. With a resistance
value of 2.2k Ω for a 12V supply, the reference voltage
has been made almost independent of load current.

Linearity of DAC is another factor affecting the
accuracy. In an ideal DAC, equal increments in the numeri-
cal significance of the digital input should yield equal
increments in the analog output. The linearity of a DAC
is then a measure of precision with which this requirement
is satisfied. Linearity is adversly affected by substan-
tial temperature changes [3].

Thus the overall accuracy and the input resolution
of the system are to a large extent dependent on the DAC
chosen. For DAC-08, the resolution is of 8 bits and nonline-
arity is $\pm$ 0.19% of full scale. With a reference voltage
of 10V, the full scale output is 9.960 volts. The output
resolution in that case is 39.8 mV. which is good enough
for the system [4].

The actual circuit of DAC-08 is described in
Fig. 2.3.3 [4]. In the diagram, R14 provides a reference
current I_{ref} to the DAC. So R14 is low temperature coeff-
icient metal film resistor (1%). In the circuit, V_{REF}=-10V
and R14 = 5.1kΩ to provide I_{ref} = 1.9 mA. I_{ref} of 1.9 mA
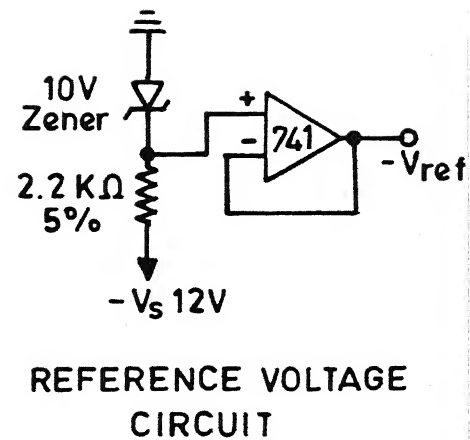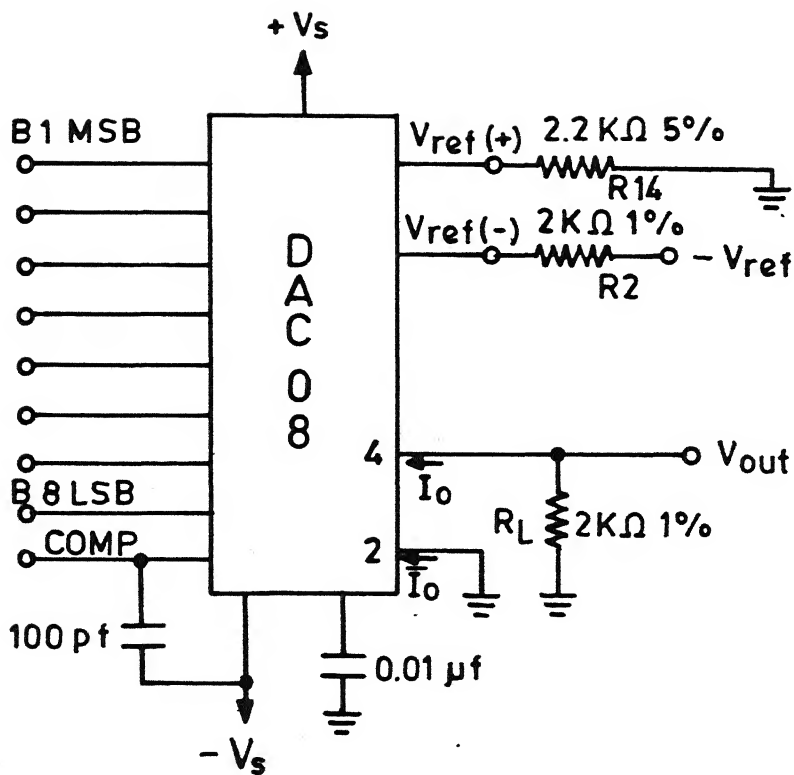
Fig. 2:3.3 Digital to analog converter operating circuitry.

is well within the specified I_{ref} range of 1·5 mA to 4 mA for DAC -O8. For R4 = 5.1kΩ, the output at pin 4 'V$_{out}$' rises from O to - 9.960 V for full scale input. Thus the output voltages of the DACs are negative.

Thus the output voltage for each channel has an absolute maximum of 9.960V, which can be easily increased by replacing the 10V zener diode by a higher breakdown voltage zener diode. For the system, however, the workstation supplies only +12,-12 and +5V, and hence it is not feasible to go beyond 10V reference .

2.3.3 Control and Switching Circuitry:

This circuitry is instrumental in providing proper signals for different types of devices, viz. BJTs and FETs. So to understand this circuitry, it is necessary to know the subtle differences between these two types of devices.

A BJT transistor is known as a current controlled device since the base current plays a significant role in its conductance. Small changes in the base current (which may be assumed to be in the input circuit for C-E mode of operation) result in large changes in the collector current (which flows in the output circuit). Thus output collector current is controlled by small input base current [5].

Furthermore, studying the I_B-V_{BE} characteristics of a BJT, (Fig. 2.3.4), it is clear that small changes in
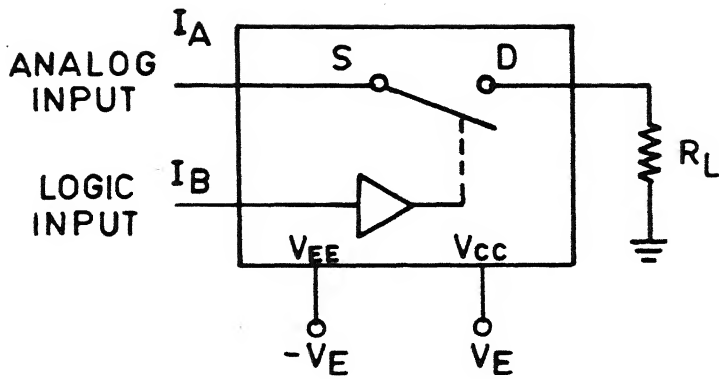
FUNCTIONAL DIAGRAM
LF 11331
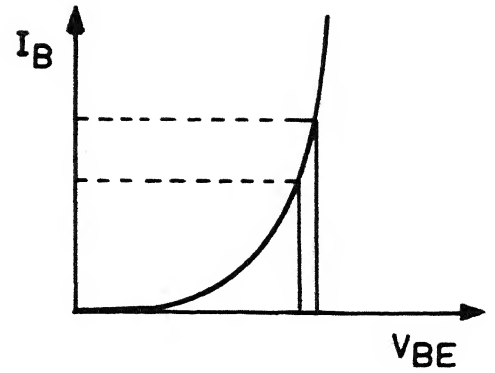
$I_B - V_{BE}$ CHARACTERISTICS
FOR A BJT TRANSISTOR

$$V_0 = -\left(\text{BUFFER 1} + \frac{\text{BUFFER 2}}{10}\right)$$
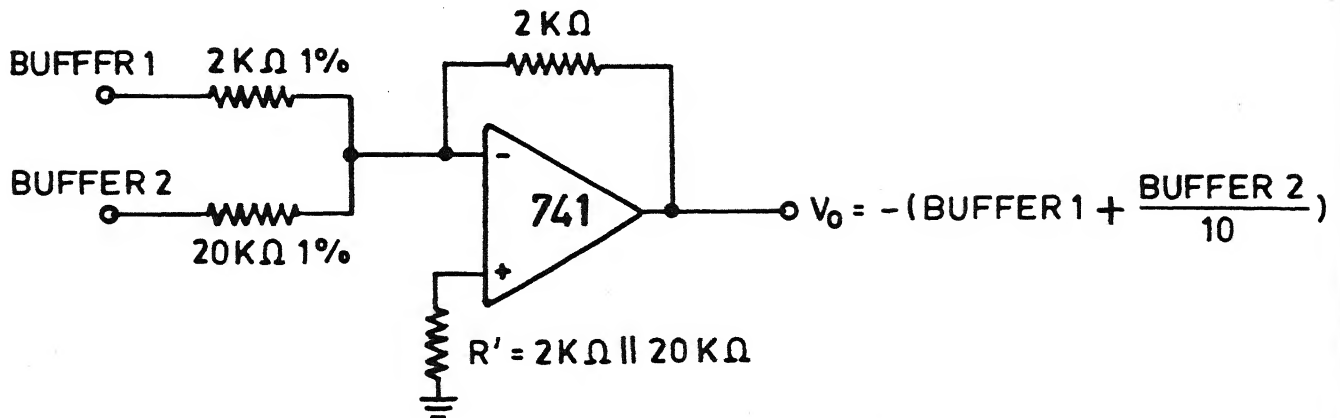
Fig. 2:3.4 Summation amplifier.

V_{BE} produce large changes in I_B in the operating region, but equivalent changes in I_B produce only moderate changes in V_{BE}. So controlling I_B becomes much more easier than controlling V_{BE} [5].

Thus a BJT is said to be a current controlled device.

Similarly for a FET (Field Effect Transistor), its structure is such that the voltage at the gate of the device and hence the ensuing electric field across the channel will control the current flowing through the drain circuit [5].

Thus while a BJT is a current controlled device, FET is a voltage controlled device. The control parameter for a common emitter configuration of BJT is I_B while that for common source configuration of FET is V_{GS}(voltage-gate to source). Moreover, polarities of all the signals reverse when NPN is replaced by PNP for BJT and n-channel is replaced by p-channel devices for FET and vice-versa.

Hence the most important task of proper test signal generation is carried out by the Control and Switching circuitry.

The signals coming from D/A data converters are buffered (Fig. 2.3.5).A fine control over I_B for BJT and over V_{GS} for FET is made possible by scaling Buffer -2 output by a factor of 10 (Fig. 2.3.4). The output equation

for the summation amplifier is $V_o = -(\text{Buffer-1} + \frac{\text{Buffer -2}}{10})$.
Thus a fine control overcoming the limitation of the DAC
resolution has now been obtained.

The switching circuit and the digital signals
controlling the switches are shown in the schematic diagram
(Fig. 2.3.5). The figure lays out clearly the method used
to change signal polarities and signal conversions for
different types of devices.

T1-T2, T3-T4, T5-T6 are complementary digital
signal pairs controlling the switches, ensuring that no two
switches at the same signal node are both open or closed
simultaneously.

Considering the case of NPN BJT, the signal at
the base is a positive current, while signal at the collector
is a positive voltage, emitter being grounded.

In the above case, T4 should be 'l', i.e. S4 is
closed to have current as input at the base (Fig. 2.3.5).
As the voltage to current (V/C) converter is a negative
converter, the input to V/C converter should be negative
for a positive current output. As the summation amplifier
output is positive, (because DAC outputs are negative), the
inverter should also come into the signal path to have
a negative voltage at V/C converter input. Thus T2 is also
'l', and S2 is closed (Fig.2.3.5).
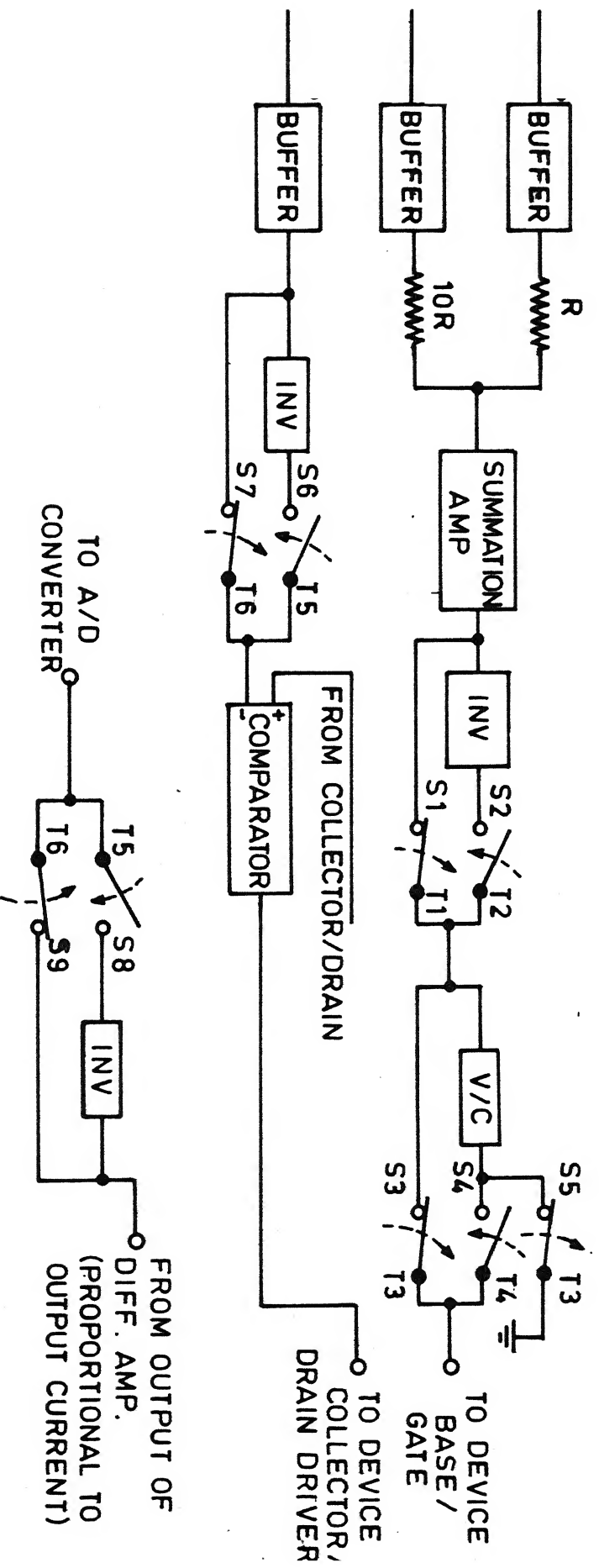
Fig. Fig. 2:3.5 Schematic diagram of control and switching circuit.

Similarly for a positive collector voltage, the inverter has to be included in the collector signal path (as the Buffer-3 output is negative). So S5 is closed with T5 = '1' (T6 = '0').

Thus for an NPN BJT, the following analog switch conditions prevail.

T2-1, T1-0	S2-closed, S1 - open
T4-1, T3-0	S4-closed, S3, S5-open
T6-0, T5-1	S6-open, S5- closed

Switches S8 and S9 ensure that the A/D Conversion module is always provided with a positive voltage.

Switch positions for different types of devices can be similarly obtained. Table 2.1 lists the switch positions for all types of devices which can be tested.

Thus by simple designing of switching circuit, a versatile setup capable of accomodating a large variety of devices has been obtained.

The function of S5 is not very obvious in Fig.2.3.5. In the V/C converter, which is a precision voltage controlled current source, the node supplying the output current builds up a high voltage if it is left open. So S5 ensures that whenever V/C converter is removed from the signal path, S5 closes and V/C output shorts to ground. Thus S5 is a very essential component of the system.

TABLE 2.1

CONTROL SIGNALS AND SWITCHES' STATES FOR DIFFERENT TYPES

OF DEVICES

Device	T2	T4	T6	S2	S4	S7, S9
NPN	1	1	O	Closed	Closed	Open
PNP	O	1	1	Open	Closed	Closed
N-MOS	O	O	O	Open	Open	Open
P-MOS	1	O	1	Closed	Open	Closed
N-JFET	1	O	O	Closed	Open	Open
P-JFET	O	O	1	Open	Open	Colsed

Note: T1-T2,T3-T4,T5-T6 are complementary pairs of signals.

2.3.4   Analog Switches Used:

LF 11331 N-channel JFET analog switches have been used for the switching of analog signals. In order that the switches do not affect the parameter under measurement ,   they should have very low 'on' resistance. This condition is satisfied by LF 11331, whose 'on' resistance is in the range of 150-200 Ω. So the choice of LF 11331 is quite appropriate [6].

The functional schematic of LF 11331 is as shown (Fig. 2.3.4). The simplicity of operation is very obvious[6].

2.3.5   Voltage to Current (V/C) Converter [7]:

This module also contributes in determining the accuracy of the system. From the analysis of the circuit of the bilateral voltage controlled current source (VCCS), it is clear that the output current is proportional to the input voltage applied. For both positive and negative input voltages, proportional current is supplied to the load (Fig. 2.3.6).

In Fig.2.3.6, the value of R5 is dictated by the amount of base current that has to be supplied. Assuming a β of 100,   and a maximum collector current of 200 mA, a base current of 2mA for V_{in}= 10V can be supplied by R5=5kΩ. The nearest value of R5 = 5.1k Ω has been chosen.

R3 2MΩ 1%

R1
2MΩ 1%

V_{in}

LM308

30pf

R2
2MΩ
1%

R4
1MΩ
1%

R5
5.1KΩ 1%

$R3 = R4 + R5$

$R1 = R2$

$I_o = \dfrac{R3\ V_{in}}{R1\ R5}$

$I_o = \dfrac{-V_o}{5.1}\ mA$
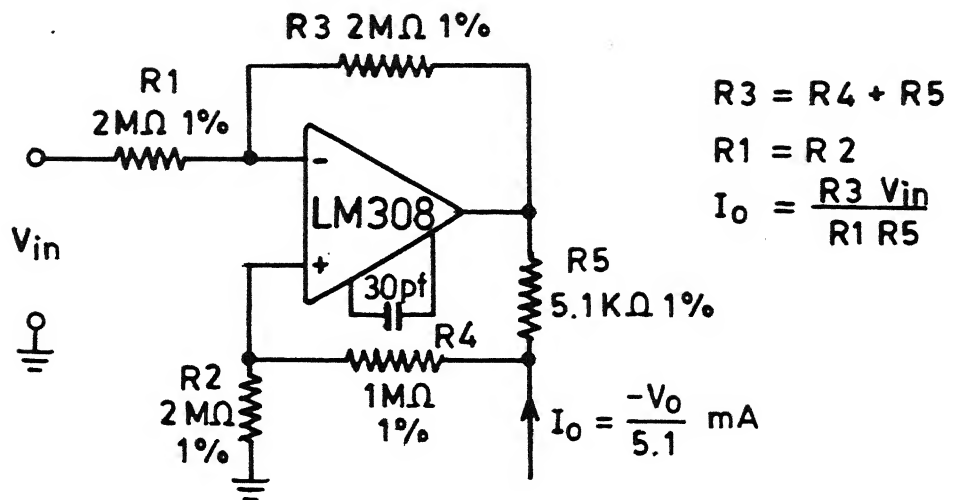
Fig.2:3.6 Precision bilateral voltage controlled current source.

R_m

D.U.T.

$+V_{CC}$

2N5294

LM308

741

2N6107

DAC 3
OUTPUT

DRIVER
STAGE

$-V_{EE}$
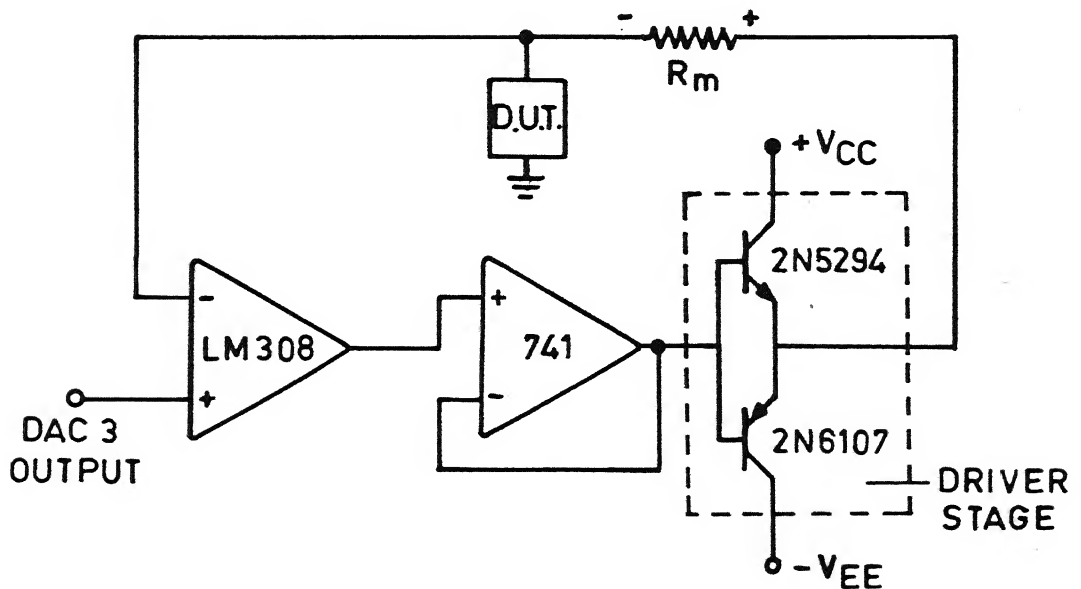
Fig.2:3.7 Collector/Drain driving circuit.

The accuracy of the converter thus directly reflects on the accuracy of the system.

2.3.6   Driver Circuit:

This driver circuit ensures adequate current providing capacity for the collector/drain current of the device under test. As such, it can be implemented by a simple push-pull configuration of a complementary pair of medium power transistors (Fig. 2.3.7).

A relevant and important aspect of the system has to be noted at this point. Channel 3 provides the independent parameter variation (collector/drain voltage control). However, to measure the collector/drain current (parameter under measurement), it is passed through a low resistor in the collector/ drain circuit and the voltage across this resistor measured. This alters the voltage at the collector/ drain of the device. This altered voltage is fed back to a comparator which compares this voltage with the desired collector/ drain voltage. This comparator output (proportional to the difference between the two input voltages) drives the push-pull stage . This negative feedback ensures that the voltage applied to the collector/drain is within 5 mV of the desired value. Thus keeping the driver stage in the feedback loop ensures proper tracking of the collector/ drain voltage.

2.3.7 Data Sensing and A/D Data Conversion Module:

This module carries out the crucial and important function of data retrieval. The importance of accurate data retrieval and conversion cannot be over-emphasised.

This module can be subdivided into two sections: Data sensing or retrieval and Data conversion (Fig. 2.3.8).

Data to be sensed can be one of the two quantities: Collector/drain current (as in I_C-V_{CE}, I_D-V_{DS} etc.) and base emitter voltage as in V_{BE}-I_B.

Collector/drain current is measured by passing it through a precision resistor and measuring the voltage developed across the resistor.

The criterion for the selection of the value of the measuring resistor is the maximum value of the current to be sensed.

The maximum input the ADC can convert is 10V. Hence the current causing the output of the difference amplifier to reach 10V is the maximum current that can be measured.

In the system, the gain of the difference amplifier in the sensing circuit is 2.94. Thus to sense a current of about 200 mA, the measuring resistor value R_m should be

$$R_m = \frac{10}{2.94 X I_C} = 18\,\Omega \text{ for } I_C=200 \text{ mA.}$$
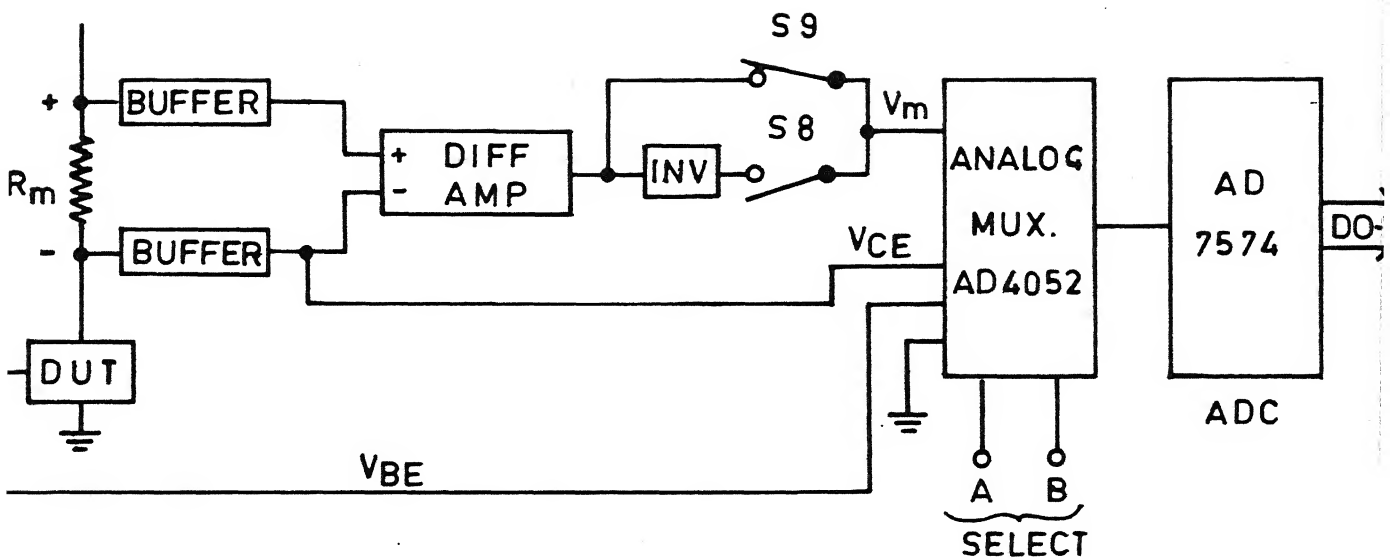
Fig. 2:3.8 Data sensing and conversion circuitry.

The value of R_m used in the system is $12\,\Omega$.

Reverting back to the main topic, another parameter worth measuring is the collector/drain voltage itself.

So the above three signals are of importance and may be required to be converted to digital form for storage in microprocessor memory.

Buffers have been used in sensing circuit so that it does not load the device.

Fig. 2.3.8 shows how all these signals are multiplexed to feed one of them as ADC input. Two 'select' inputs A and B do the channel selection in AD4052 analog dual 4 i/p multiplexer. A and B are treated by the selection logic as two output ports (Table 4.1). The AD4052 is an easy to use chip. The channel resistance is very low and hence it does not affect the parameter under measurement.

The AD4052 output is then fed to AD7574 ADC as analog input.

AD7574 is an 8 bit ADC. it is the most important link in the data measurement path since it is solely responsible for converting data to digital form to be passed on to the workstation. Thus the accuracy of the ADC data conversion is very important. So it has to be very carefully designed. The circuit diagram is as given in Fig. 2.3.9 [8].

It is essential to know about AD7574 and its various operating modes to understand the design.

a)   Static RAM Interface Mode [8]:   In this mode, a conversion start is initiated by a WRITE to the ADC. Converted data is read by executing an ADC READ. Thus two separate commands have to be given for complete conversion. Moreover, the time delay between the WRITE and READ has to be software controlled. So this mode is not fit for application in the measurement system.

b)   ROM Interface Mode [8]: In this mode, $\overline{CS}$ is held low and converter operation is controlled by the $\overline{RD}$ input.

This mode is simple to operate. The major disadvantage is that the data obtained is poorly defined in time inasmuch as executing a data read automatically starts a new conversion cycle. So this mode has not been used in the system.

c)   Slow Memory Interface Mode [8]:   In this mode, $\overline{CS}$ and $\overline{RD}$ are tied together. Conversion is initiated by READing ADC. $\overline{BUSY}$ subsequently goes LOW, placing the microprocessor in the WAIT state (as $\overline{BUSY}$ is connected to READY). The $\overline{BUSY}$ goes HIGH when the conversion is over, completing the ADC READ.

The major advantage of this mode is that it allows the microprocessor to start conversion, WAIT, and READ data with a single ADC READ. Thus this mode has been

used for data conversion in the system.

The selection logic generates the $\overline{CS/RD}$ signal to start the data conversion. $\overline{BUSY}$ is connected to the workstation READY input [8].

The ADC has an internal asynchronous clock oscillator which starts upon receipt of a convert start command and ceases ocillating when the conversion is complete. The clock oscillator requires external R and C. The values of these are decided from conversion curves provided for the ADC. In the case of the measurement system, the values are as follows: C= 100 p.f. and R= 120kΩ[8].

The ADC is operated in a unipolar binary mode i.e. the output binary data increases monotonically in numerical significance with the increase in analog input. This is very convenient and hence is preferred over the Bipolar (Offset Binary) operation mode.

The quantization error or relative accuracy error of the ADC is $\pm$ 3/4 LSB. In order to minimize the effect of this error, the software carries out averaging by reading the output four times. The conversion time with R=120kΩ and C = 100 p.f. is approximately 15 μ secs.

Thus ADC 7574 is a very crucial link in data retrieval and accurate data conversion. The data read from the ADC is stored by the software in the microprocessor memory.

All the hardware described above, when put toge-
ther, buildsup a comprehensive data measurement system. In
particular, DACs, analog switches and ADC are very important
in enhancing and maintaining the accuracy of the system.
However, all other elements are equally important for proper
functioning of the hardware.

2.4 ALTERNATE PHILOSOPHY: ADVANTAGES AND LIMITATIONS:

All along, the information that the system retrieves
or uses is in the quantitative domain rather then temporal
domain. It is a well known fact that better accuracy can be
obtained for measurements of temporal quantities rather than
quantities like voltages and currents. Hence an obvious
alternative to measurements of currents and voltages is the
measurement of time, a property of which can be modulated
by voltage in many different ways.

One of the methods is to use Pulse Width Modula-
tion (PWM). This principle will give an output whose
width is proportional to the input voltage. Then the width
of the pulse can be measured using a high frequency clock
along with a digital counter. The counter, when enabled for
the output pulse duration width, will give a count proportio-
nal to the voltage input. The higher is the frequency of the
clock, the better is the resolution of the measurement.

This count can then be compared with some standard
count for a stardard input and the output magnitude of the
quantity measured obtained.

The obvious advantage is that the accuracy of the output measurement now depends largely on the high frequency clock selected . Better resolution can be obtained by simply changing the clock frequency. Moreover, the advantage accruing from noise immunity (because of the digital nature of the circuit) will be immense. Furthermore, it is not necessary to have a hardware clock. Software clock can also be implemented using microprocessor interrupts.

The main disadvantage of the system will be the amount of time required for each conversion. The higher the quantity (voltage) to be measured, more is the time taken for measurement because the pulse width increases and hence more conversion time will be required. Moreover, the information stored is also in terms of counter counts, which has to be converted to meaningful output. Further processing of the information (which is essential) will thus involve arithmetic operations such as multiplication/division. Hence a lot of time will be consumed in just processing the retrieved data . Hence the system will be essentially slow.

Another disadvantage is the additional hardware required for the pulse width modulation. Moreover, the conversion of pulse width to a clock count in hardware will entail additional hardware. Carrying out the process in software will further slow down the system response.

Thus it can be concluded that if just accuracy is the criterion without much regards to speed and increase in hardware complexity, the pulse modulation approach is more suitable. But in cases where the accuracy required is not very critical, conventional voltage measurement approach is more practical and desirable.

CHAPTER III

SOFTWARE DEVELOPMENT AND IMPLEMENTATION

It may be said of any kind of action that the action itself, as such, is neither good nor bad. If it is done rightly and finely, the action will be good, if it is done basely, bad.

:- PLATO

3.1 INTRODUCTION :

A system using hardwired logic to perform specific function is self sufficient in operation. It can perform the intended function without external aid . However, any changes in the scope of or functional capabilities of such a system have to be accompanied with redesigning of some or whole of the hardwired logic.

A system using a microprocessor as its processing unit, on the other hand, can adopt to the changes in its definition with minimal hardware changes. This is due to the capability of microprocessors to respond differently to different instructions given to it.

This set of instructions which operates the whole system centered around a microprocessor is known as software.

No hardware by itself can perform any moderate-sized operation efficiently. Just microprocessor based hardware without any software to operate it is meaningless.

Even though the hardware performs the primary task of data collection, the software that controls it really defines the system [11].

It can be said that while hardware is the tool utilized by a designer to carry out a task, software is the expression of the designer as to how the tool should be utlised. Software reflects the notion of the designer about how efficiently and effectively can the resources at hand be utilized. It also decides how closely can the user come to defining his problem accurately.

In the case of the measurement system under study, all the hardware has to be controlled so that under different circumstances, the hardware does the desired distinct operations. This is because the system tries to incorporate all types of devices along with a variety of tests for each device.

Software development for the measurement system has been carried out using PL/ M 80, a Higher Level Language[10]. This has been done for better user–system interface and in view of complexity of the programming involved in the case of the measurement system. PL/M 80 is exclusively developed to simplify the programming of Intel 8080/8085 microprocessors. Further details about PL/M 80 are given in Appendix II.

3.2   IMPLEMENTATION OF SOFTWARE:

The basic flow chart of the software of the system is as shown in figure 3.2.1.   The different modules in
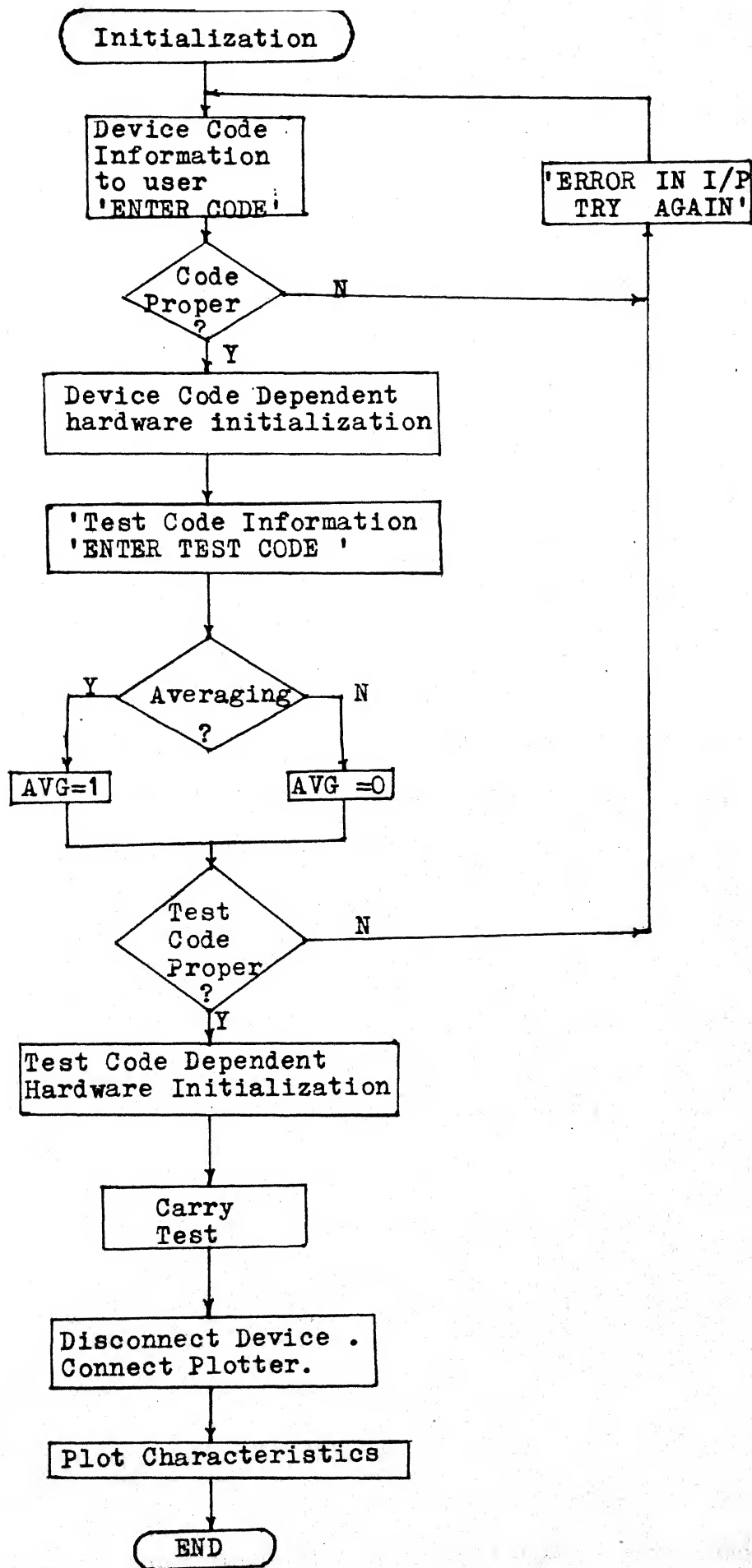
OVERALL SOFTWARE FLOWCHART
Fig. 3.2.1

the software have to be implemented using different algorithms.

The first task performed by the system software is the initialization of all the flags and ports used by the system. These flags are set or reset according to the desired initial conditions.

The system software indicates completion of initialization by a message 'SYSTEM READY'.

The user is informed about the device types handled by the system and the device code associated with each device. The user inputs the code of the device type to be tested. The software checks the input for any error in the code and, if so, prompts the user to try again. This and such other features of the system make it user friendly.

With the device code input, hardware initialization takes place. The analog switches are set or reset to ensure that proper types and polarities of signals will be applied to the device. The DACs are also initialized so that their quiesent state initial outputs will not take any device into conducting state. For example, in its non conducting state, a JFET (Junction Field Effect Transistor) has a high voltage at its gate. So this takes care of the hardware initialization. Now the system is ready for testing a device.

For any type of device, a variety of tests are available for different characteristics of the device. Moreover, some tests can be performed only on a particular type of device.

For example, $I_B - V_{BE}$ test can be performed only for a BJT. Similarly, $I_D - V_{GS}$ test can be performed only for a FET. Software informs the user about the type of tests available. These tests are software controlled and they comprehensively test the device for that particular type of characteristics. Additional information on each test is given in Appendix III.

The test code input by the user then decides the way DAC1 and DAC2-3 will be used. For example, during $I_C - V_{CE}$ test on BJT, DAC1 will vary over O-OFFH for each value of control parameter I_B, which is now controlled by DAC2-DAC3. Similarly, for $I_B - V_{BE}$, V_{CE} is the control parameter. So now for each setting of DAC1, DAC2 will vary over O-OFFH range. Thus software makes use of test code for identifying the control parameter and the independent parameter.

The software then invokes the routine used for conducting the actual test on the device. The device undergoes the test and the measured quantity as well as the independent parameter are stored in the memory along with each control parameter value.

Any measurements or characteristics derived without provision for a hardcopy are useless. The purpose of the system as a quick and easy tool for determination of characteristics will then be defeated. So some hardcopy interface has to be provided.

Moreover, the information stored in the memory is in binary form. The software retrieves this information and presents it in a readable form.

An X-Y plotter interface has been provided to tackle this problem of hardcopy output. After device test is over, the software uses DAC2 for X-axis output and DAC1 for Y-axis output. Before the software starts driving DAC1 and DAC2, the user is informed to remove the device and connect the plotter X -axis input to the Base/Gate terminal and Y-axis input to the Collector/Drain terminal. This approach saves a sizeable amount of hardware for the plotter interface.

Software then plots the characteristics on the plotter for different values of control parameter. In order to have minimal user interaction, the retrace of the X-Y plotter is also controlled by the software. The value of the control parameter for which the characteristic is currently being plotted is displayed on the video terminal.

Now each software module will be studied separately

3.3 SOFTWARE AND HARDWARE INITIALIZATION:

Before the operation of any system begins, it is very essential that the system be in a known state. In our system, both the software flags and the hardware ports are set or reset according to the desired initial condition.

Software flags are defined for (a) type of device, (b) test code,(c) error message etc. Hardware ports

to be initialized consist of DAC1, DAC2 and DAC3. These are also initially set to zero.

After the device type information has been given to the user and the device code entered by the user, further hardware initialization takes place (Fig. 3.2.1). This initialization sets analog switches appropriately so that proper types of signals are provided to the device (Table 2.1). The DACs are also appropriately initialized. For example, in the case of a JFET, the gate has to have a high voltage for it not to conduct. So DAC2 and DAC3 have to be set 'high' when device code indicates PJFET or NJFET. Similarly for a BJT device, the Voltage to Current converter is to be connected in the base/gate signal path. If any erroneous input is given to the system, software flags an error message and waits for proper input.

3.4 TEST CODE INFORMATION:

Test information is provided to the user through series $\underset{\wedge}{\text{of}}$ messages. These messages spell out the possible tests that can be carried out by the system.

The test code entered by the user also does some further initialization. The test code determines whether the base/gate parameter is going to be the control parameter and collector/drain the other independent parameter or vice versa. This is done by setting or resetting a flag 'CD'. For example, in the case of Test 1 i.e. $I_C - V_{CE}$ in the case of BJT

[see Appendix III], I_B and hence base/gate parameter is the control parameter and V_{CE} is the other independent parameter. Then CD=0. But in the case of Test 2, i.e. $I_B - V_{BE}$, V_{CE} is the control parameter and I_B is the variable parameter. In this case, CD =1. .

So the software takes care of the above detailed aspect while carrying out the indicated test on the device.

Similarly, a flag 'ACD' is present which indicates whether or not a JFET is being tested. This flag is set or reset immediately after the device code has been entered. Thus flags 'CD' and 'ACD' completely specify the analog switches setting and the control parameter.

These two flags make it possible to design just one software routine which can be used to carry out different types of tests on different devices. The routine has been described in detail later.

3.5 AVERAGING INFORMATION:

As has been indicated earlier, the Analog/ Digital Converter AD7574 has a conversion error of $\pm$ 3/4 LSB. So to eliminate this conversion error, and some error due to slight variations in the input to ADC, averaging function is desirable. This has been implemented in software by averaging over four consecutive readings. However, averaging takes place only if the user so desires.

3.6 ROUTINE FOR DEVICE TESTING:

The flow-chart for this routine 'ON' is given in Fig. 3.6.1.

This algorithm is the single most important algorithm as all the different test routines use this basic routine for testing purpose by appropriately setting the parameter list of this routine.

Examining the routine closely, it can be seen that throughout this routine, the value of BASEDR , which is to be the value of the control parameter,is constant. Another routine 'ONB', described later, invokes this routine 'ON' for different values of control parameter. This 'ONB' has 'k'=O for the first value of the control parameter. 'k' is acting as an index to the independent parameter buffer array 'Y' and to the array 'Z' storing the measured parameter value. So data retrieval after the test becomes easier.

'CD' and 'ACD' are used for proper driving of the device under operation and putting it off when nc test is being conducted. To understand the use of software delays and interrupt disables 'used by the routine, the following discussion is essential.

In any measurement system, it is essential that the validity of the parameter under measurement should not suffer due to the measuring test itself. In the case of a BJT,

K: Index of buffer storing the independent and measured parameters

$Y(K)$: Element in array 'Y' Storing the kth value of the independent parameter
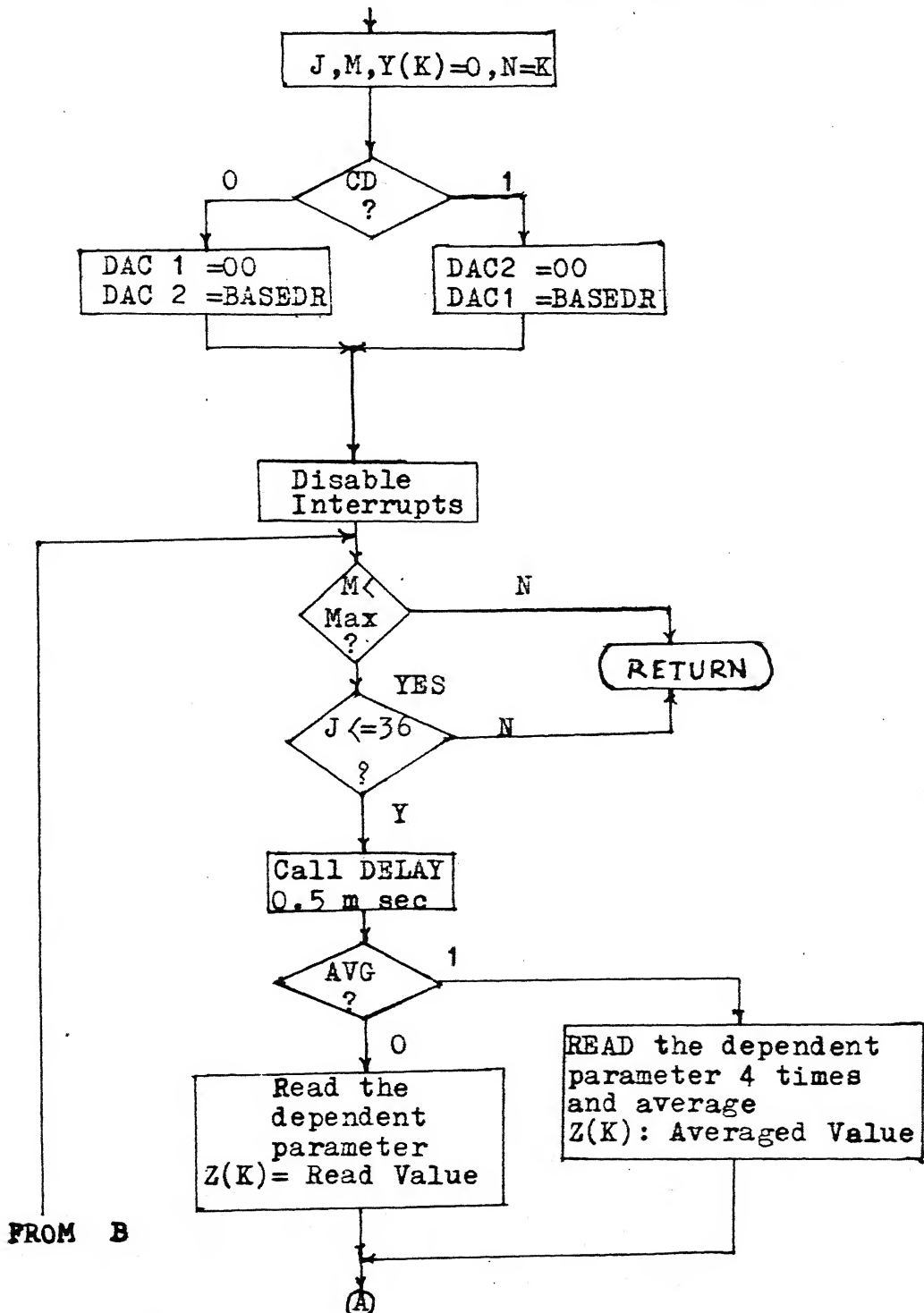
$Z(K)$: Element in array 'Z' Storing the kth value of the measured parameter

BASEDR: Value of Control parameter

M : Value of the independent parameter in a particular iteration

AVG : Flag indicating whether averaging to be done or not

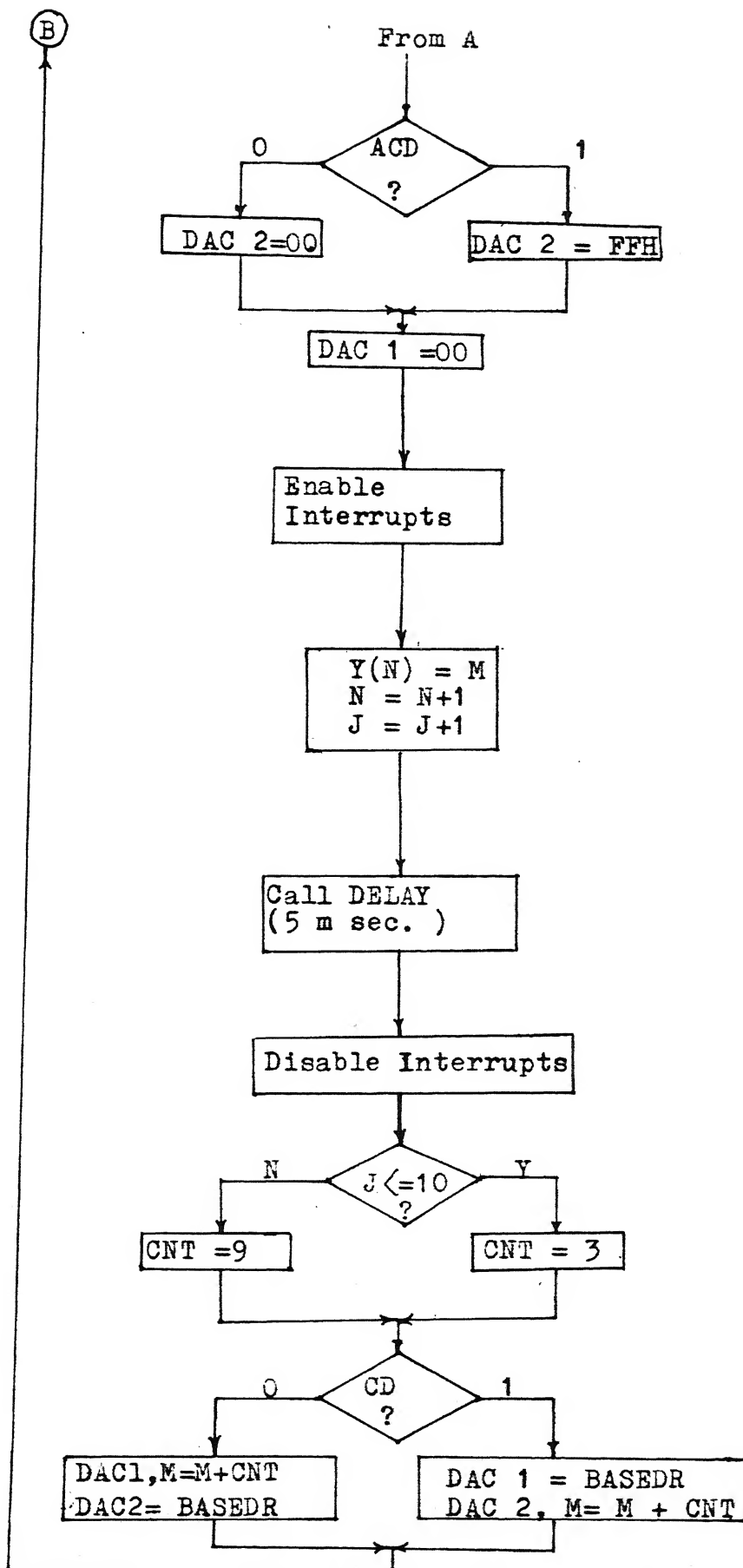MAX : Max value that the independent parameter can attain.

FROM B

Fig. 3.6.1   (Contd..)

applying base current at high collector voltage for long
enough time may increase the internal temperature of the
device enough to invalidate the measurements. Particularly,
in small transistors, base currents inducing high collector
currents, if allowed to flow for 1/100th of a second, may burn
out the transistor. Determination of high collector currents
for high collector voltages or base currents requires turning
the transistor on for a very short time with a low duty factor.

Such temperature effects have to be avoided [2]. The
routine 'ON' handles this by applying the voltages and currents
to the device in pulses 0.5 msec. wide. The dependent parameter
is allowed to stabilize and then measured at the end of the 0.5
msec period. These short pulses are generated by the software
using ' Delay ' routine.

Before the application of signals,interrupts are
to be disabled so that even if an interrupt is being requested
during measurement, it will be serviced only after the measure-
ment has been made and the stimuli to the system removed.
Otherwise, if the device is being driven while an interrupt
is encountered and serviced, the device may get damaged.

Immediately after the measurement is made, the
stimuli to the device are removed and the interrupts enabled .

A software delay of 5 msec. is then activated
before the independent parameter is incremented , and the
stimuli again applied to the device for the next measurement.

This ensures that the duty cycle of the device is less than
0.1 and hence no heating of the device takes place.

The routine 'ON' tests the device for only one
value of the control parameter. For different values of the
control parameter, i.e. for different values of BASEDR in 'ON',
we get   different sets of measurements. Thus the control
parameter variation has also to be carried out for complete
characteristics.

Routine 'ONB' carries this out by testing the
device for different values of control parameter (Fig.3.6.2).

As can be seen, for each value of N in the
routine (N is acting as control parameter value and is applied
to appropriate D/A converter), the routine 'ON' is invoked
once. Moreover the value of 'k' (index to independent para-
meter array 'Y' and measured parameter array 'Z') is initi-
alized to 'O' only once at the beginning of 'ONB'. After each
iteration in 'ONB', 'k' is incremented by 36. This ensures
that for each value of control parameter, the set of 36 values
of independent parameter and dependent parameter are stored
contiguously right after the previous set of these values for
the previous value of the control parameter. This allows easy
retrieval of data as and when required.

Figure 3.6.3 shows the train of pulses that will
be generated for different values of the independent parameter
for successively increasing values of the control parameter.

in memory.

ITR : The number of characteristics plotted by the routine .

TH : Threshold value of the control parameter used for first iteration (User Stored at 5000H)

INC : Stored at 5001H. **Added** for BJT, Mosfet (ACD =0)
Subtracted for PJFET (ACD≐ 1)
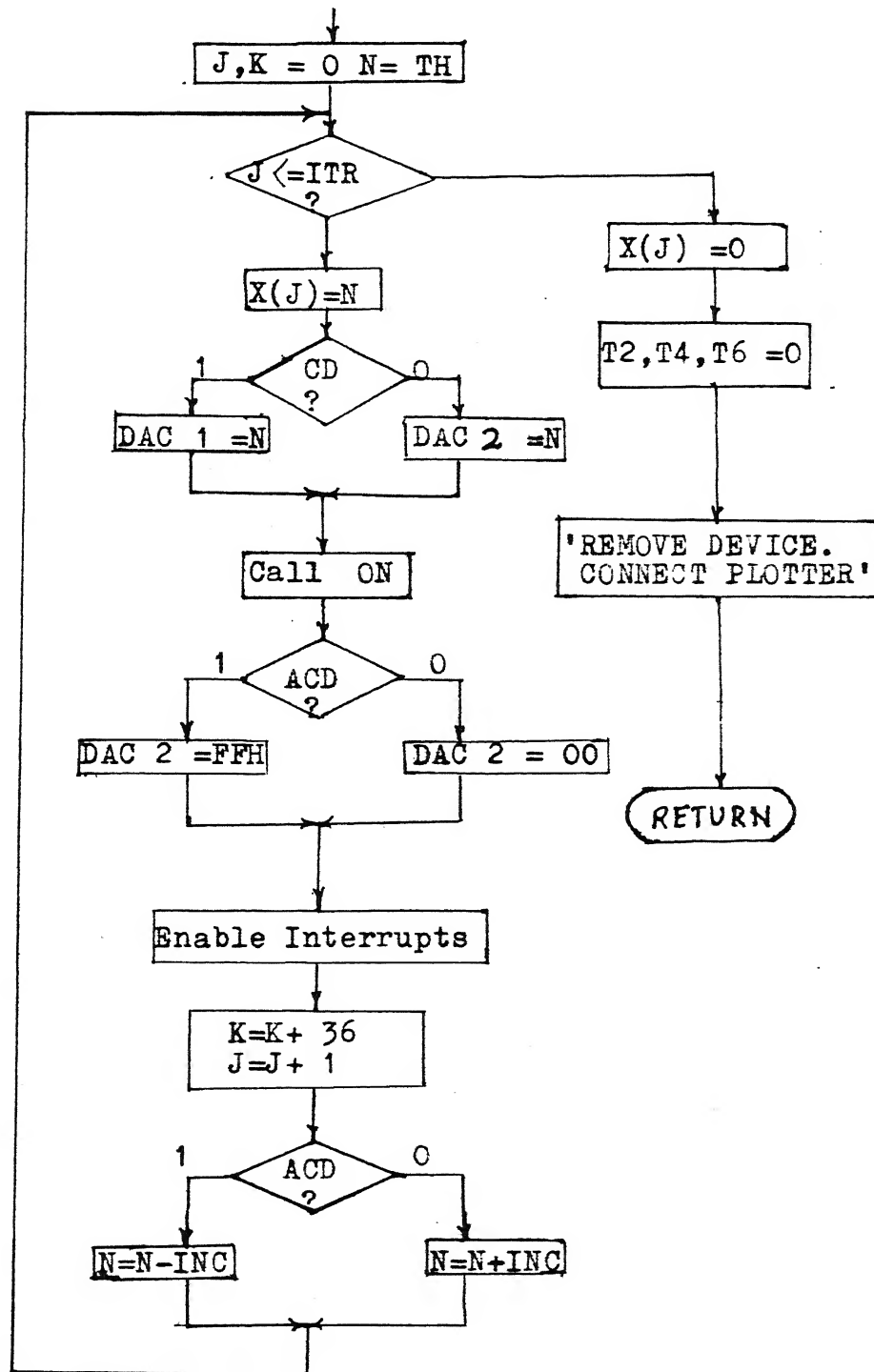
FLOW CHART FOR ROUTINE
'ONB'

Fig. 3.6.2

Fig. 3:6.3 Pulses genenerated during 'ONB'.

Another important feature to be noted is that, depending on 'ACD', the control parameter is incremented or decremented after each iteration. It is decremented in the case of a JFET because JFET conduction decreases for higher values of the gate voltage than for lower values.

The values of 'TH' (Threshold) and 'INC' (Increment) for the control parameter are to be stored by the user in memory locations 5000H and 5001H respectively.
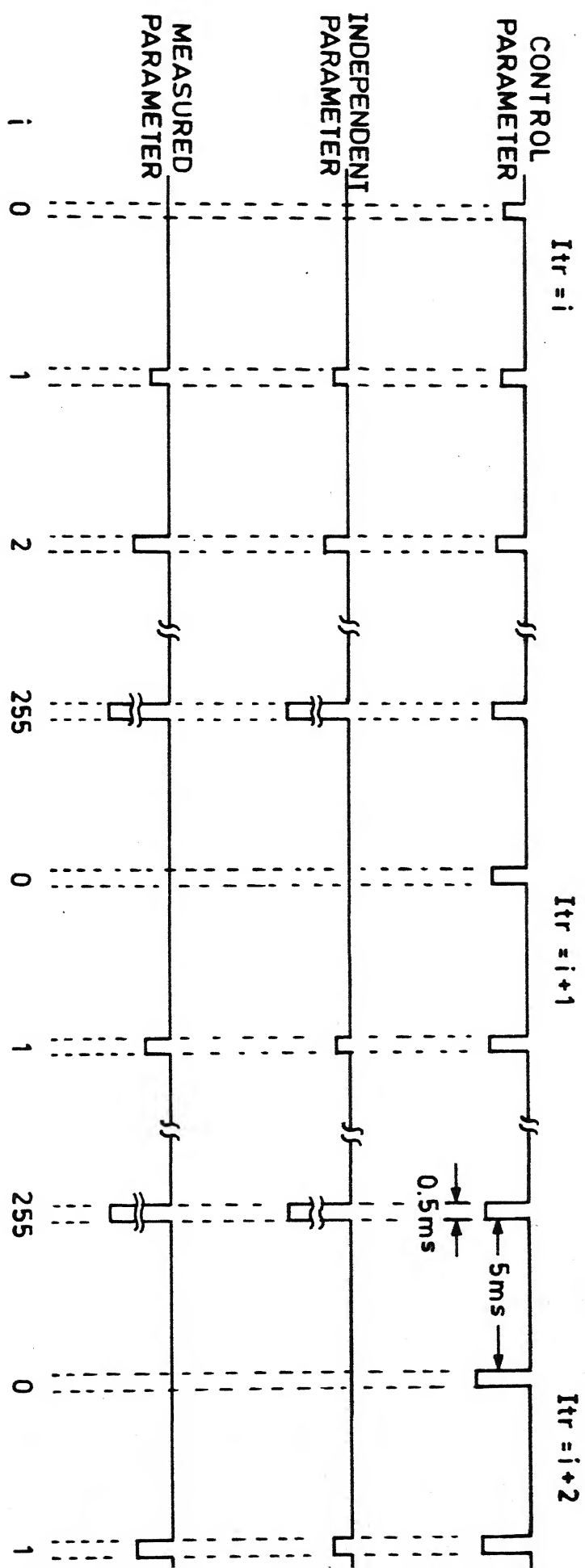
After all the iterations in 'ONB' are over, the hardware has to be now initialized to connect the plotter for hardcopy. The analog switches are set so that outputs at X and Y inputs of the plotter are positive voltages.

DAC2 is treated by software as X-axis output while DAC1 is treated as Y-axis output. The software gives a prompt to remove the device and connect the plotter after the hardware has been reconfigured for plotter operation.

Figure 3.6.1 shows, how, for each value of control parameter, the increments in independent parameter are affected. It can be seen that for a lower value of the independent parameter ('J' is its index), the increments are low. This is to have better resolution in the saturation region (near origin) where the changes in the current I_C/I_D with respect to V_{CE} are much more than those in active region. Thus for each value of control parameter, there are 36 various independent parameter values at which measurements are made.
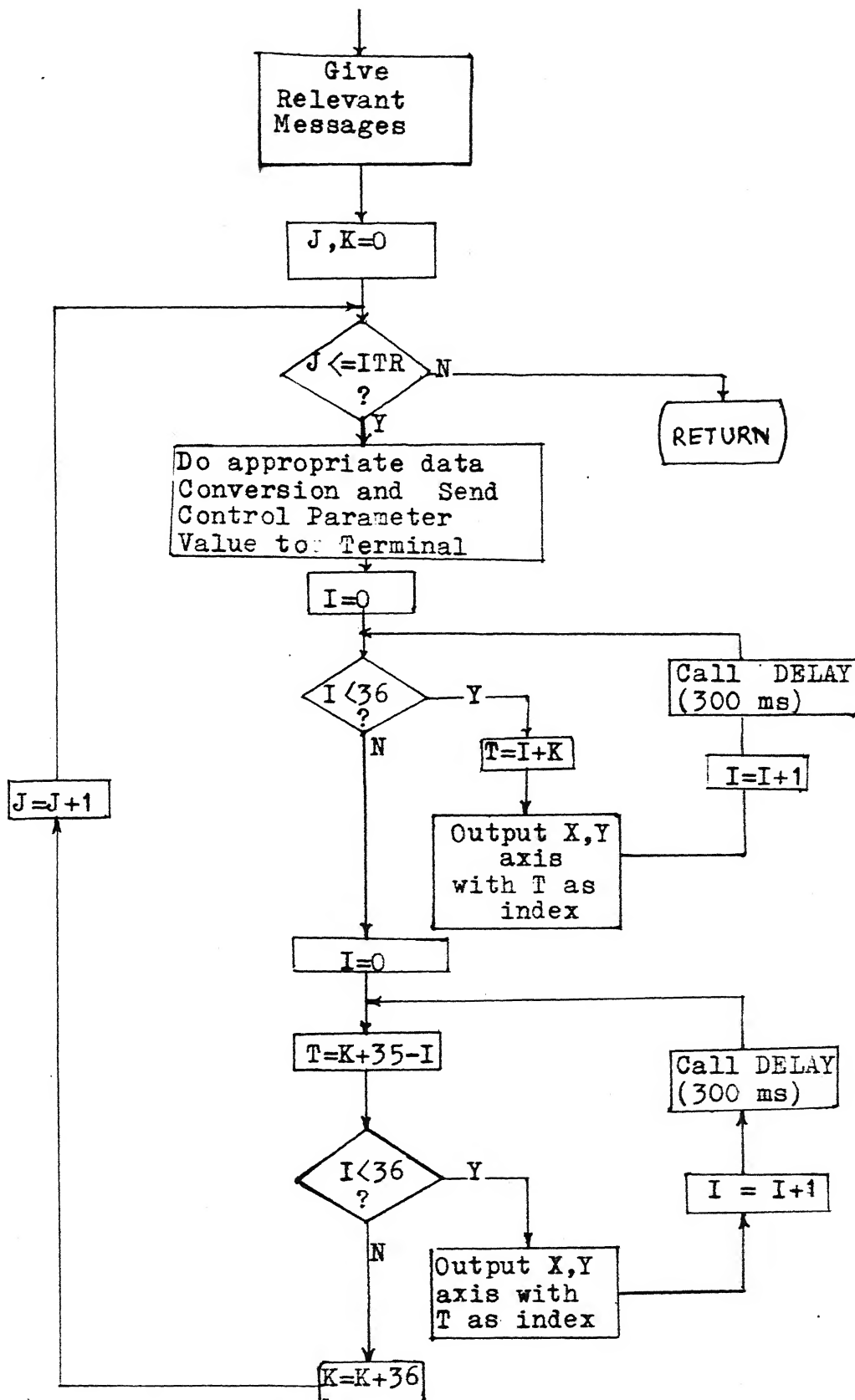
X-Y PLOTTER OUTPUT
FLOWCHART

Fig. 3.7.1

3.7 OUTPUT FORMATTING ROUTINES:

Depending on the device type and the test carried out on the device, the measured parameter and the control and independent parameters are interpreted differently. Also, output scaling has to be done in some cases as the data may not be appropriate for plotter representation.

The proper data conversion and outputting to X-Y plotter is done by ' OUTP' and 'OUTP1' routines. These routines act differently for different tests. This is because the different tests have different control and independent parameters and hence stored in different buffers. So they have to be interpreted accordingly.

For different values of control parameter, the output to X-Y plotter is for different plots. The values of the control parameter for corresponding plots are output by the software to the video terminal.

For minimum user interaction, the X-Y plotter, after plotting a plot, automatically retraces to origin before the next plot is drawn. This helps in making the system automatic and user friendly.

The flowchart for the output algorithm is as shown in Fig. 3.7.1. The time delays of 300 msecs. netween two consecutive outputs to the X-Y plotter is to adopt the speed of the output to the speed of the plotter. Scaling

factors have been used in some cases for better readability
of the characteristics. For example, in the case of $I_B - V_{BE}$,
maximum value of V_{BE} is about 0.8V. for silicon transistor. So
the V_{BE} axis has to be modified for better readability.

3.8 CONCLUSION:

It is seen that throughout the software design,
an attempt has been made to automate the whole system oper-
ation with just the least amount of user interaction. The
software has been successful in doing so .

An efficient code has also been obtained for the
software by developing a few basic routines which can be
run for different devices under different test conditions.

CHAPTER   IV

INTERFACE OF HARDWARE AND SOFTWARE

4.1   DESCRIPTION:

The Hardware and Software of the system descri-
bed perviously have to be interfaced properly for the
desired operation of the system.

The software of the system has been developed,
as mentioned earlier, using PL/M 80 Higher Level Language.
This has been developed using Intel Microprocessor
Development System ISIS Series III machines.   The code
generated after compilation of the program is stored in
an EPROM whose location in the workstation memory address
space is from 6000H to 6FFFH.   The data buffers used to
store the values of different parameters during measure-
ments and the software flags storing the status and the
information input by the user are located in RAM area of
the workstation.   For the workstation, RAM is mapped from
4000H to 57FFH.

The Data buffers have been addressed in the
software from 4000H to 4500H. The software flags have been
stored from 5100H onwards.

The stack segment for the software starts from
5FE0H downwards.

Thus the hardware selection logic should do address decoding so that the EPROM address 'select' is present only from 6000H to 6FFFH addresses. All the addresses decoded for the system hardware are decoded by the Selection Logic.

When the software is run, the microprocessor jumps to location 622CH (where the first executable instruction of the code resides). The microprocessor then reads the instructions and executes them. Thus the micro-processor operation is now being controlled by software stored in the EPROM.

The software treats all the analog switches, DACs and the ADC as input / output ports. The addresses are generated by the system hardware selection logic.

The analog switches are driven by flip – flops which are treated as input/output ports (Table 4.1). The M.S.B.of data bus is present as the data input to the flip-flop. Thus, if a particular filp-flop is to be prog-rammed as '1', the data bus should have M.S.B.high.

The memory map and the input/output location map for the system hardware is given in Table 4.1. While deciding the memory and input/output port address locations, the memory map and I/O map of the workstation has been taken into consideration and care has been taken so that no overlapping of address takes place.

TABLE 4.1

MEMORY AND I/O MAP FOR THE MEASUREMENT SYSTEM

MEMORY MAP

ADDRESS	MEMORY
6000-6FFFH	INTEL 2732 EPROM
5000H	'TH'
	PROGRAMMED BY USER
5001H	'INC'

I/O MAP

ADDRESS	OUTPUT PORT
00H	DAC1
01H	DAC2
02H	DAC3
10-1F	T6(T5=$\overline{T6}$)
20-2FH	T2(T1=$\overline{T2}$)
30-3FH	T4(T3=$\overline{T4}$)
70H	A
	SELECT Inputs for AD4052
71H	B

ADDRESS	INPUT PORT
40-4FH	ADC(AD7574)

Thus the interfacing of software and hardware ensures proper functioning of different hardware components and software operating on them.

CHAPTER   V

TEST   RESULTS AND CONCLUSIONS

5.1 INTRODUCTION:

Commenting on the performance of any system requires the proof of how accurately does the system carry out its intended function. In the measurement system developed here, some sample tests have to be carried out before its accuracy and flexibility can be compared . An attempt has been made in this direction. Tests have been carried out on different types of devices and results compared with the ones directly obtained. This comparison helps in estimating the accuracy of the system.

Such comparison also helps to analyze the short-comings of the system and to overcome them for improving the performance of the system. The following section discusses the results of the tests conducted on the various types of devices. It also compares these results with the results obtained directly and comments on the accuracy of the system.

5.2 TEST RESULTS:

Test results have been carried out for all types of devices for obtaining I_C-V_{CE} or I_D-V_{DS} characteristics. The devices tested were NPN 2N5249, PNP SK100B, PNP CIL157, N-channel MOSFET CD4007 and P-channel JFET 2N4221. The

characteristics for each device will be studied separately.

Fig. 5.2.1 shows the NPN 2N5249 I_C-V_{CE} characteristics. As has been already pointed out, readings for 36 different values of V_{CE} between 0-10V have been taken for each value of I_B. So the whole characteristic has been defined by 36 discrete points over the 0-10V range. This explains the wavy nature of the characteristics. A bias has been introduced near origin for plotting more points to get better resolution (see section 3.6). However, as all the characteristics are crowded near origin, these characteristics have been approximated by smooth curves near origin for the sake of clarity. As can be observed, these curves are almost equally spaced for equal changes in the base current I_B.

Verification of these curves for 2N5249 has been done and the results show that variation from actual characteristics is about 5%. While measuring the accuracy of the system, ten points on characteristics have been taken and compared with the actual values of the parameter of interest at these points.

This variation of 5% is due to some inaccuracies in the system hardware. The first and obvious source of errors are converters. As has already been pointed out, the DAC outputs are very sensitive to the reference voltage given to them. Similarly ADCs also use a reference voltage for
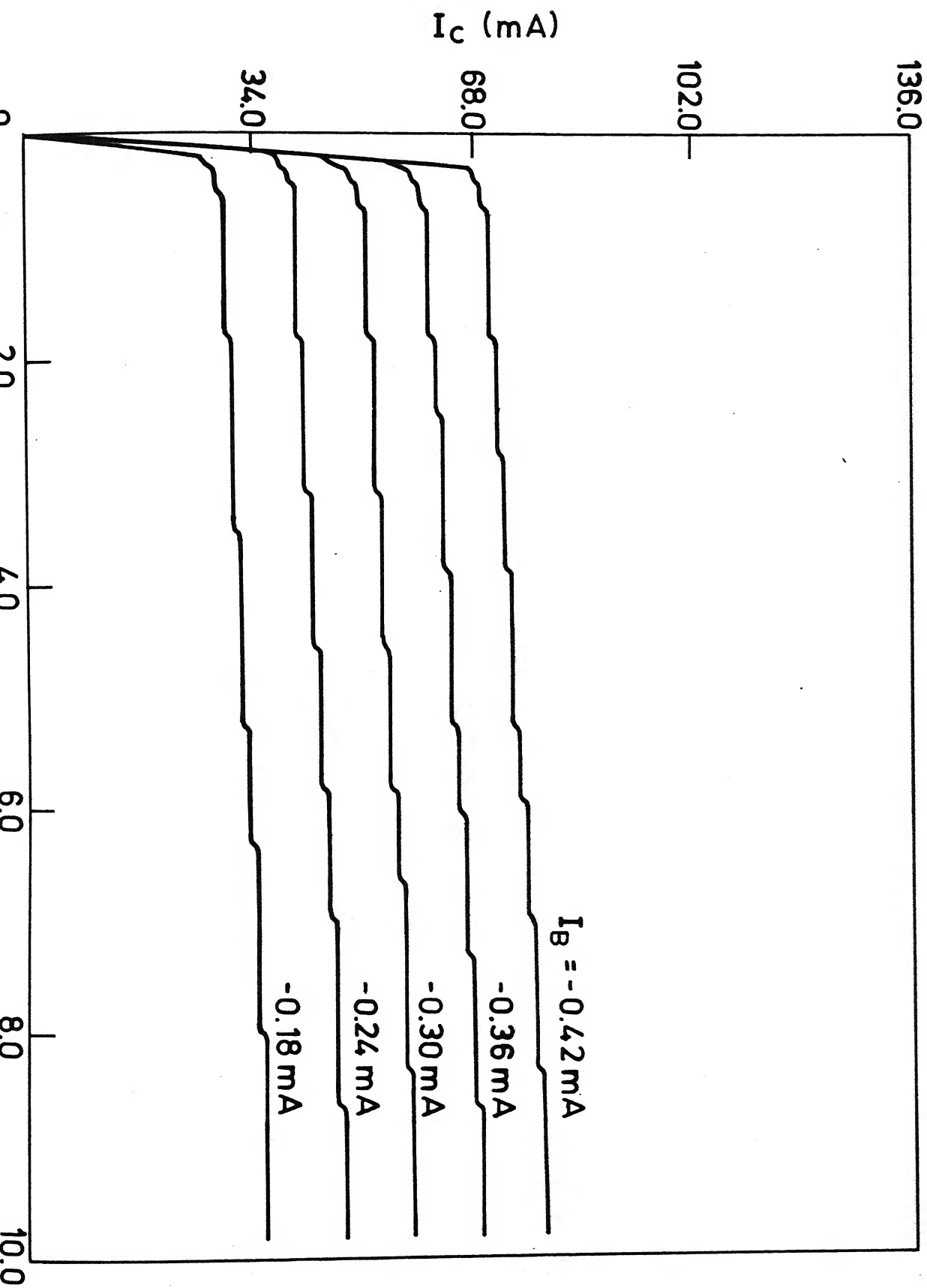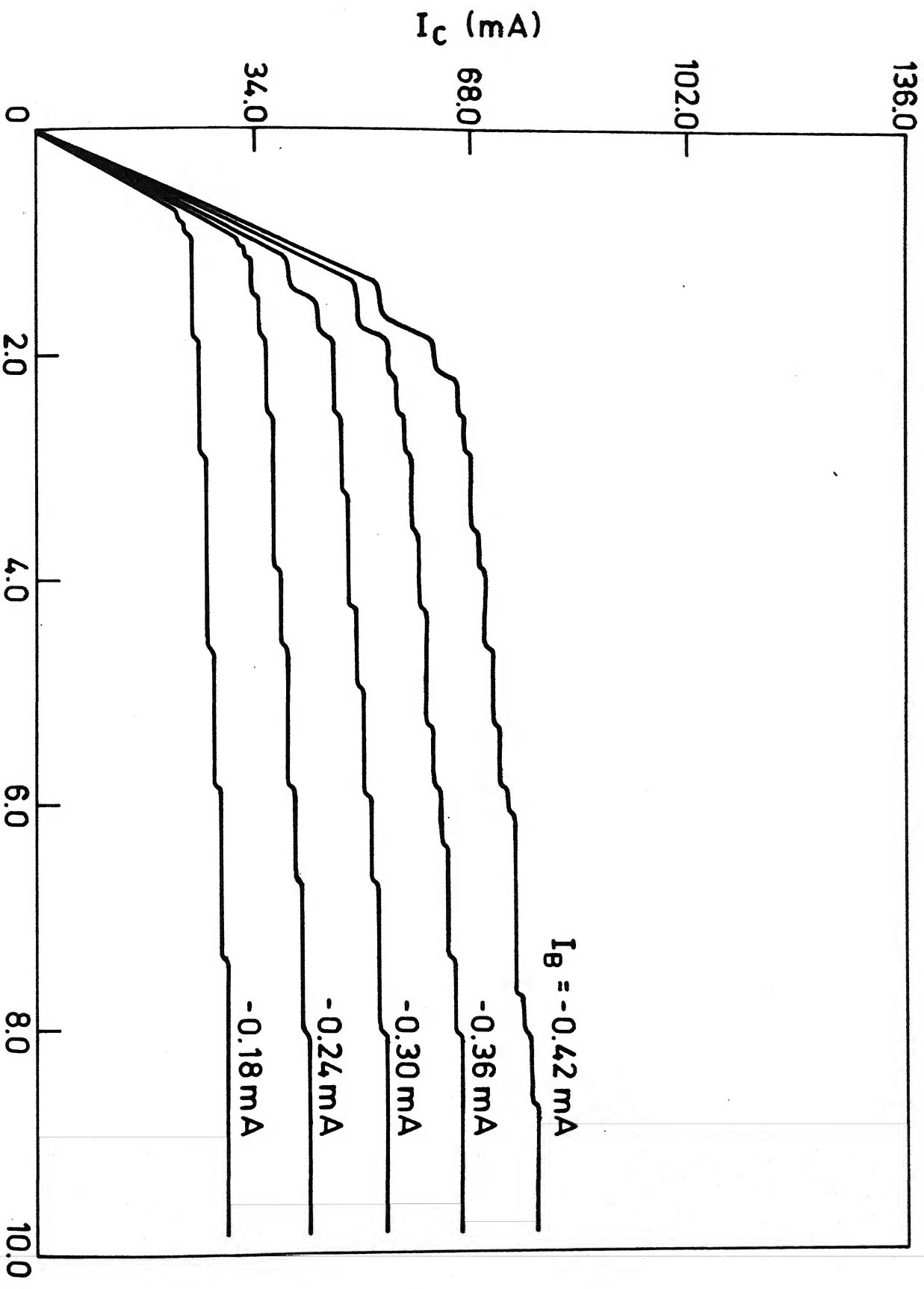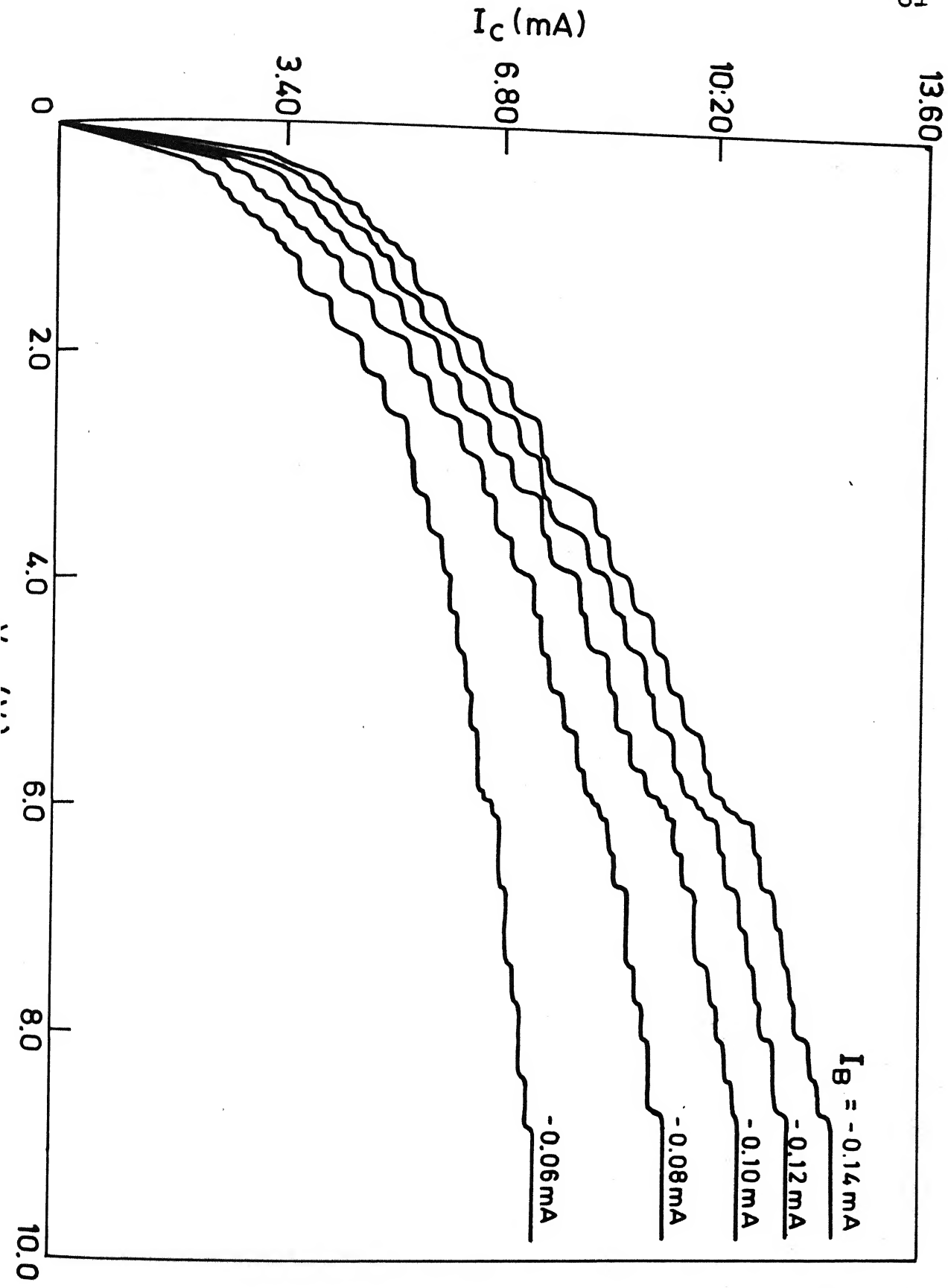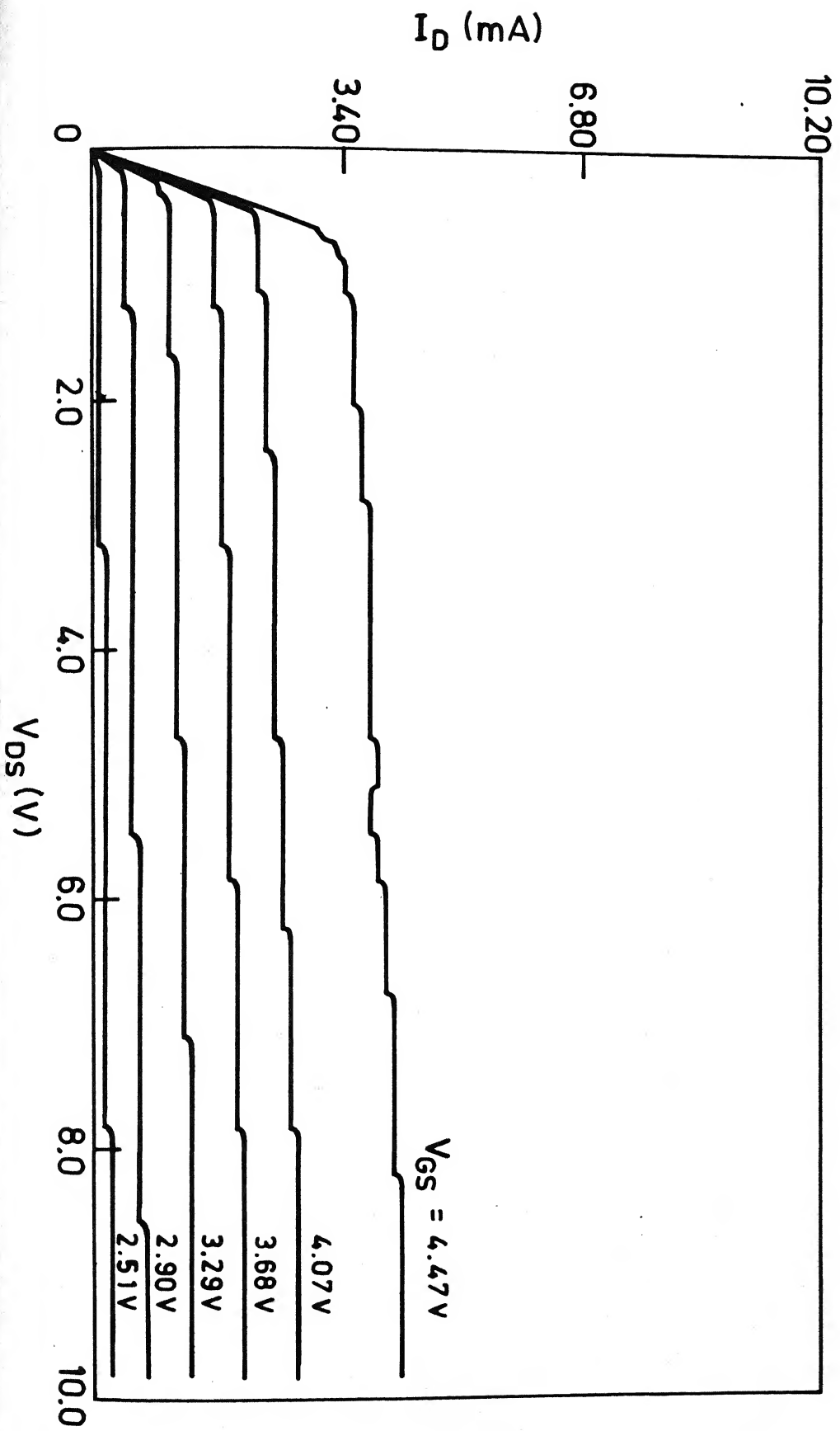
conversion. Hence the precise value of the reference voltage and its variation assumes a lot of importance.

In this system, a simple zener diode with 10V breakdown voltage has been used. The breakdown voltage of a 10V zener diode, unfortunately, is not precisely 10V but has some err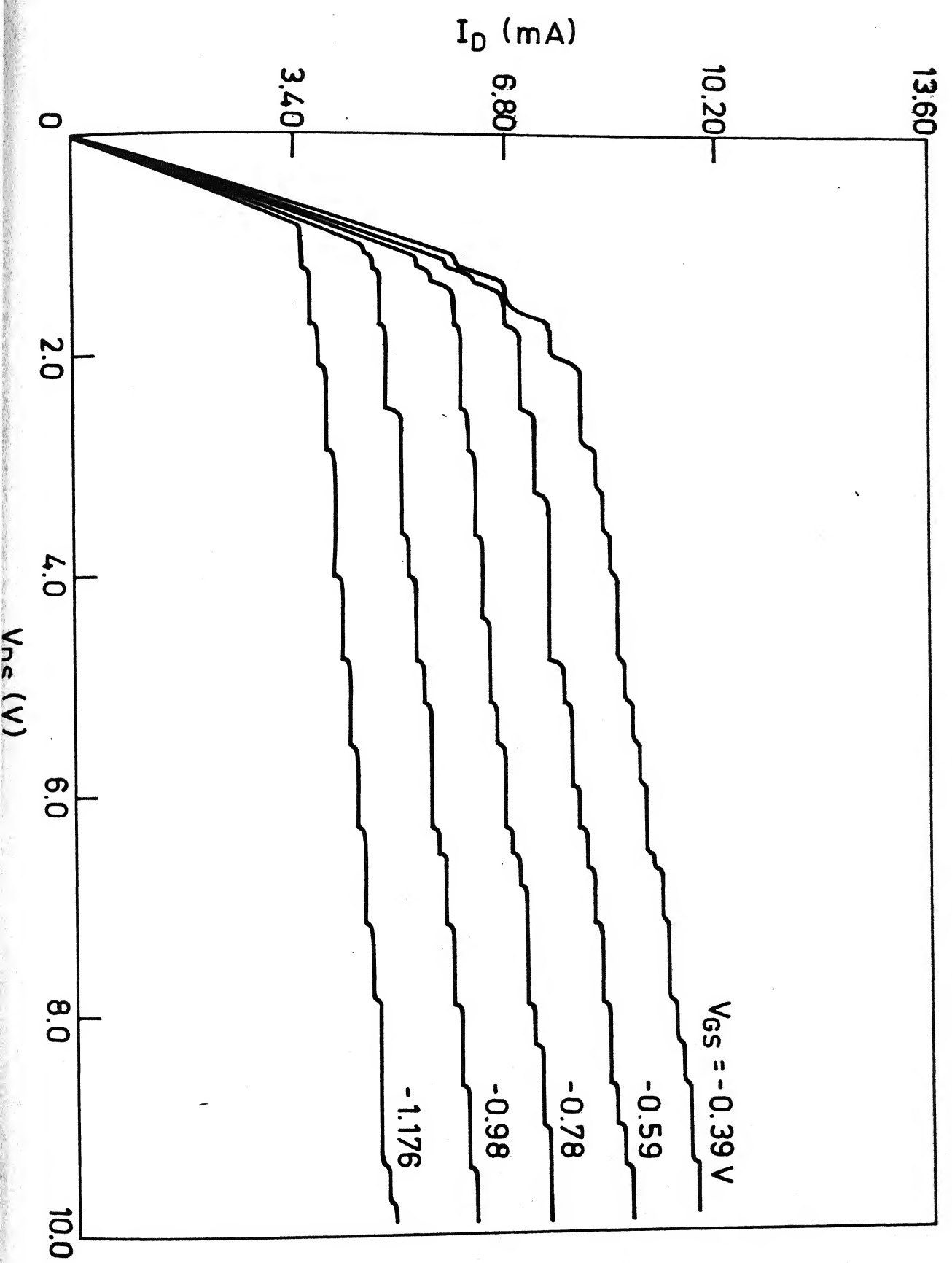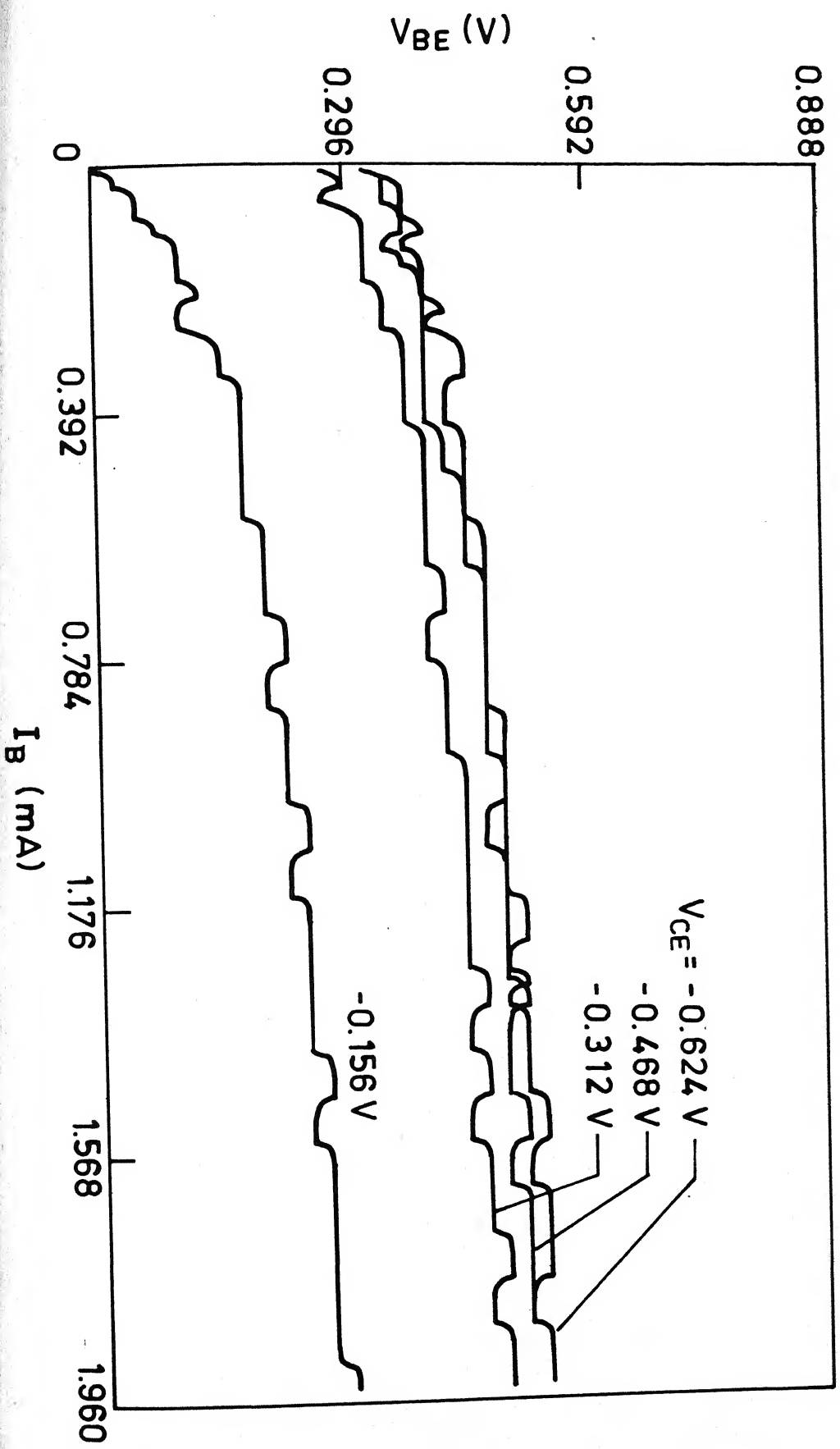or in it. Moreover, no temperature compensation has been provided for the zener reference used. This reflects directly on DAC as well as ADC conversions. These errors are mainly responsible for the 5% error that is present.

To overcome this limitation, precision 10V voltage reference IC AD584 can be used. This IC also has almost zero temperature coefficient. This IC has been specifically designed for use with converters. It is also easy to use.

Another possible source of error may be the difference amplifier used to measure voltage across the resistor in the collector circuit. In this stage, all the errors of two voltage follower buffers, one inverter and the difference amplifier creep in and hence a small error is introduced at this stage also (Fig. 2.3.8).

Characteristics have also been obtained for other devices. Fig. 5.2.2 and 5.2.3 show the I_C-V_{CE} plots for PNP SK100B and PNP CIL157. It can be seen that the two devices have clearly different regions of operation.

SK100B is a medium power transistor while CIL157 is a
low power transistor.

This wide range of currents can be handled only
if there is some mechanism for switching of scale by switching
of the measuring resistor R_m' (2.3.8). However, in the
measurement system, this has not been implemented. The two
characteristics for these two transistors have been obtained
by physically replacing R_m' (12Ω) by a different resistor
(120Ω for CIL157).

This situation can be overcome by two pairs of
analog switches which will switch the two resistors depending
on the magnitude of the collector/drain current. This scale
switching can be controlled by software.

The error in PNP SK100B characteristics is in the
range of 4.7%, but that in the case of PNP CIL157 is more. This
may be because of the fact that the higher the resistor
in the collector/drain circut is, the higher is the absolute
error in the voltage developed across it. This directly
affects the accuracy of the measurement.

Figures 5.2.4 and 5.2.5 show the I_D-V_{DS} plots
for N-channel MOSFET in CD4007 and P-channel JFET 2N4221
respectively. The errors found in the case of P-channel
JFET 2N4221 are 4.7%. These are as a result of a high
value of resistor used in the collector circuit.

Figure 5.2.6 shows the V_{BE}-I_B characteristics of SK100B PNP Germanium transistor. These characteristics are obtained for different values of V_{CE}. The abscissa is the base current I_B, while the ordinate is the base emitter voltage V_{BE}.

The plots have been shown only for four values of V_{CE} because for higher values of V_{CE}, the plots do not vary much as that from the highest V_{CE} shown in Fig. 5.2.6. Moreover, the plots are as expected because increasing V_{CE} with constant V_{BE} decreases the base width W_B and results in decreasing recombination current.

It is seen that the V_{BE}- I_B characteristics are of more wavy nature. This is because the value of V_{BE} for Germanium transistors is very low. For appropriately presenting V_{BE} values to X-Y plotter, it has been magnified 5 times by software routine 'OUTP1'.

The error in V_{BE}- I_B is about 5%. The error is small enough taking into account the fact that the very small values of V_{BE} correspondingly reduce percentage resolution of the ADC.

Other tests offered by the system can similarly be run and test results obtained for them.

All the above obtained characteristics show that the system is moderately accurate with a variation of about 4%.

To sum up the reason for errors, these errors have a source in the reference voltage that has been given the DACs and ADC. A better reference voltage scheme will be to provide this precision voltage through a precsion reference IC AD584.

Another source of error can be the difference amplifier stage which senses the voltage across the collector/drain current measuring resistor R_m. This can be corrected with the help of offset compensation circuit.

5.3 FURTHER SUGGESTIONS AND CONCLUSIONS:

One major limitation of the system is that the maximum voltage at the output of the three DACs is 10V. This is because of the reference voltage of 10V. This limits the output of DACs to 10V maximum. This is a limitation for some devices which are operated near 15V.

Also, ADC cannot sense any voltage beyond 10V. This limitation can also be overcome by increasing the reference voltage. However, one major feature of the system has been that it has been designed to operate only with the help of workstation without the help of any external power supply. This restricts the supply voltage to 12V provided by the workstation, thus making any other higher reference voltage for the converter infeasible.

Another point to be noted regarding software is that, the software is quite involved. So the machine

code generated is about 4k bytes. As the hardware board has provision for just 4k bytes of ROM memory, no further software expansion is possible at present. However, with additional memory, the system software can be made very exhaustive and elaborate. Routines for extraction of secondary information from characteristics already obtained (such as V_{cutin} for $V_{BE}-I_B$ for BJT, V_{TH} for I_D-V_{GS} for FET etc.) as also for further tests on devices (such as r_d-V_{GS} for FET) can be incorporated. This will help increase the scope of the system significantly.

Dividing the whole range of the independent parameter values in just 36 discrete points impedes the system performance to a certain extent. However, 36 readings for each of the different control parameter values will occupy a lot of memory space in RAM. In order to reduce the amount of memory used, a trade-off has to be effected. However, care has been taken to see that very less important information is lost. As there is much more variation of the dependent parameter near the origin in any characteristics (saturation region) than in active region, the saturation region has been covered quite well by the software by having about ten readings in this region.

The system, at present, handles devices in common emitter/common source configurations. On a broader scale, the system software and hardware can be appropriately

modified to handle the common base/common gate and common collector/common drain configurations for the devices also. This will increase the scope of the system significantly.

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APPENDIX I

MICROPROCESSOR WORKSTATION

The Microprocessor Workstations have been designed to enable users to develop software in the assembly language of the 8085A microprocessor and use such software for real-time control of any target hardware. Each workstation essentially consists of an 8085A based microprocessor kit, various interfaces for digital as well as analog input/output, and a video terminal (TTY) for user interaction. The (ASCII) keyboard as well as the video monitor is controlled by a separate 8085A processor, which reads characters from the keyboard, sends them serially to the main 8085A processor via an RS232C link, and displays the characters received from the main processor via the same serial link. This display processor has its own 2k byte RAM for storing the characters constituting a 25 X 80 characters page displayed on the CRT screen. The main processor has associated with it 16k bytes of EPROM (4 X 2732) containing the Monitor, Editor, Assembler and other system Routines. These EPROMS occupy the address space 0000-3FFF (Hex) in the Memory Map. The system has 8k bytes of RAM (16 X 2114) occupying the address space 4000-5FFFH. Addresses from 5800H to 5FFFH are used for the stack and the scratch pad requirements of the system routines, and as such the address space 4000-57FFH is available for users.

All relevant pins of the main processor, including the data
bus and the demultiplexed address bus, have been made access-
ible to the user at a 44-pin edge connector, so as to permit
memory as well as I/O expansion.

APPENDIX II

INTEL PL/M 80 SOFTWARE DESCRIPTION [10]

PL/M 80 is a high level language exclusively
developed to simplify the programming of INTEL 8080/8085
microcomputer systems. Along the lines of the Fortran IV
and PL/1 high level languages, by using structured design
techniques for writing correct programs, the PL/M compiler
facilitates the automatic control of the internal registers,
main memory, and stacks, and external memory and peripherals
in disk and tape operating systems via input/output interface.

The PL/M compliers look after the details of mach-
ine and assembly language programming, while the programmer
concentrates on the effective software and logic design. The
PL/M compilers are written in ANSI standard Fortran IV.

Salient features of the PL/M are as given below
1. A sequence of declarations and executable statements
make the program.

2. The declarations allow the control of memory allocation
and define simple textual macros and procedures.

3. The procedural facility reflects modular programming as
a sectional division into subprocedures such as keyboard
input, binary-to-decimal conversion, and output printing.
The subprocedures facilitate easy formulation and debugging,

and make a convenient libary for direct incorporation into other programs.

4. The data are made up of (1) BYTE, variable or constant, as an 8-bit identity and (2) ADDRESS, variable or constant, as a 16 bit (2-byte) word.

5. The executable statements specify computation such as arithmetic, boolean algebra, and operators BYTE and ADDRESS for comparison.

6. Conditional tests, branching, loop control, and procedure invocation with parameter passing make similar statements. Basic I/O statements to read and write BYTES to and from the microprocessors are defined as built-in procedures in PL/M 80.

7. For readability, explanation and Documentation, a comment in the form shown is permissible.

```
/* THIS IS A COMMENT */
```

APPENDIX   III

DEVICE   TESTS

Test 1 :   This test is used to find out the I_C/I_D-V_{CE}/V_{DS}

characteristics.

The control parameter in the case of BJT is I_B

and that in the case of FET is V_{GS}.

The characteristics are plotted for 7 different

values of the control parameter.

Initial value (threshold) of the control parameter

is taken from 5000H and increment for the control

parameter after each iteration is stored in 5001H.

Initial values and increments are stored in digital

form.

For BJT, OFFH for control parameter gives I_B-1.9mA.

For FET,OFFH for control parameter gives V_{GS}=10V.

V_{CE}/V_{DS} vary from 0 to OFFH.

Test 2 :   (BJT ONLY).

Used to find out V_{BE}-I_B characteristics.

The control parameter is V_{CE}.

The characteristics are obtained for 7 different

values of the control parameter.

The threshold for the control parameter V_{CE}=0V.

Increment is of 0.16V.

I_B varies from O to OFFH (O-1.9 mA).

Test 3: (FET ONLY)

Used to find out I_D-V_{GS} characteristics.

The control parameter is V_{DS}.

The characteristics are plotted for 7 different values of the control parameter.

Thereshold value of the control parameter is stored in 5000H and increment for the control parameter is stored in 5001H.

V_{GS} varies from O to OFFH.

Test 4: Used for β/g_m-I_C/V_{GS} characteristics.

The control parameter is V_{CE} in the case of BJT.

The control parameter is V_{DS} in the case of FET.

The characteristics are plotted for V_{CE}/V_{DS}=1OV.

In the case of BJT, I_B varies from O to OFFH (O-1.9 m

In the case of FET, V_{GS} varies from O to O8OH.